MICROCOMPUTER BASED SYSTEM FOR SEMICONDUCTOR DEVICE CHARACTERIZATION

By

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to the

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Dedicated to

my school teachers

CERTIFICATE

This is to certify that the thesis entitled, 'MICROCOMPUTER BASED SYSTEM FOR SEMICONDUCTOR DEVICE CHARACTERIZATION' is a record of work carried out under our supervision by Shri S. Chandrashekhar and that it has not been submitted elsewhere for a degree.

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S. Chandrashekhar

ABSTRACT

A Microcomputer based system has been designed and implemented for fast and accurate measurement and recording of I-V characteristics of semiconductor devices. The System will find application in a process monitoring section of any device manufacturing organization.

The system is designed to work in conjunction with Intel 8085/A based workstations or 8085/A microprocessor Kits. The system is modular in the sense that it is built from three independent functional modules namely, driver, sensor and the memory block. And, it can be interfaced with any 8 bit micro-computer with suitable interfacing circuitry. The system is made powerful and userfriendly. The device type, current and voltage ranges are selected through Keyboard-Video terminal interface. The execution of the process is fully under the control of the user through the Keyboard. The results are displayed on the screen and are stored in the memory. The V-I characteristics are simultaneously plotted with the help of a X-Y recorder interface.

The system has been successfully tested for PN Junction diodes like LEDs, Solar cells, Zeners and three terminal devices such as SCR, BJT etc. and their characteristic curves are obtained.

The V-I characteristics of solar cells are obtained under different illuminations and the parameters namely, open circuit voltage, short circuit current, maximum power, fill-factor, voltage, current, efficiency and R_{out} at maximum power are obtained for different illumination intensities. These values are stored in memory and displayed on the screen.

The tests have yielded good accuracy over the entire range and it can be improved further by going in for DACs and ADCs of higher resolution.

A proposal has been made for setting up of a computer-aided device testing facility.

CONTENTS

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

The advent of computers has revolutionised the field of industrial control, instrumentation and system design. The mini and micro computers have become inexpensive enough to bring the power of digital computing to the fields where it had not been possible previously.

The microcomputers have especially found many applications in dedicated systems. The power of Instrumentation System has been enhanced and its stability improved to a great degree. Also, the system has been rendered more flexible than ever before. Several layers of software reside in the memory of the computer, the lower ones nearer to the machine and the upper ones more easily accessible to the human operator. Several tasks previously handled by hardware are more elegantly accomplished by the resident software, automated measurement and recording being a good example.

The work presented in this thesis was taken up as a first step towards setting up a computer-aided semiconductor device testing facility. This system will be very useful

for the semiconductor device manufacturing organizations where it can be utilized for quick checking of the device characteristics and an extended use may be made for device process monitoring. Besides this, the system also serves as a forerunner to setting-up of a Master Control facility in an Electric Power System where the main task of running the system, consists of monitoring the voltages and currents.

It is hoped that in a few years time the goal will be achieved with the advent of more powerful and versatile microcomputer systems. It is also envisaged that with the advancement of technology we will be able to use higher level languages on the microcomputer, which are used very sparingly on them at present. With this the power of the system will be enhanced considerably. And, with the help of additional hardware and software the system may be made capable of extracting device parameters for CAD simulation packages.

1.2 ORGANIZATION OF THESIS

In chapter 2, the various components of a microcomputer based data acquisition system are discussed. Working principles of DACs, ADCs, S/H circuits etc.. are outlined. The microprocessor work station is described with the help of

schematics. The particular components selected are also described along with some application notes.

In chapter 3, the functional modules making up the system are described. Finally, in this chapter the overall system is examined.

In chapter 4, various tests and results of solar cell characterisation, LED/Diode/Zener, SCR testing etc., are explained.

In the concluding chapter 5, the present system is critically examined and suggestions for further improvements are made. A computer-aided device testing facility is proposed for further investigation.

CHAPTER 2

COMPONENTS OF DATA ACQUISITION SYSTEMS

2.1 INTRODUCTION

This chapter deals with the various components of the data acquisiton system. The important components are the data converting devices and peripheral interfacing circuits, which serve to establish an interaction between the digital domain of the computer and the analog world.

There is a wide variety of microcomputers and data converters to choose from, so as to suit our requirements. The selected components are briefly described in the following pages. Here we must not fail to recognize that in some cases the availability of components plays more vital role than its complete suitability in the selection of components.

2.2 DIGITAL TO ANALOG CONVERTERS

The basic equation governing the D/A converters can be written as $y = K \times A \times B$

y = analog output voltage or current

K = constant (generally unity)

A = analog reference voltage or current

B = applied binary word (n bits).

Fig. 2.1 shows the basic block diagram of a DAC system. A precision D.C. reference power supply forms the analog reference source. This should be capable of producing a precise voltage or current reference. There are basically two variations in this unit. In some cases it may be packaged inside the DAC package or in other cases it may be external to the DAC. The DACs using external reference are termed multiplying DACs. In some DACs both options are provided. The second block is the current output resistor ladder circuit . The two types of networks employed are Binary weighted resistor type and R-2R type. The DAC resistor ladder takes the binary input word, and gives a current output proportional to it and the reference signal. The schematic diagrams of weighted resistor and the R-2R are shown in Figs. 2.2 and 2.3, and are self-explanatory.

The binary weighted resistor becomes unsuitable if the bit length is large, because the currents due to least significant bit becomes very low and it is difficult to find an opamp to handle such low currents. Further, the range of resistor values becomes very large and unsuitable. The solution to this is the R-2R ladder, for which only two values of resistors need be used.

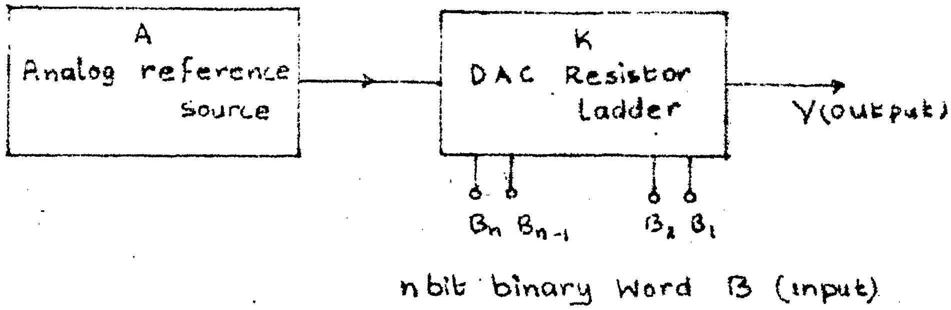
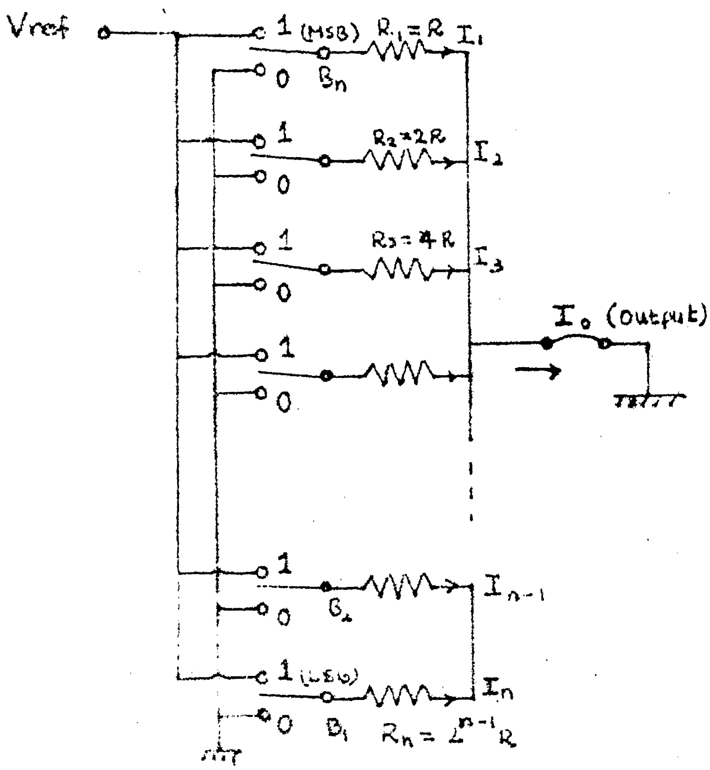


Fig 2.1 Basic DAC system



$$I_o = V_{ref}\left[\sum_{1} \frac{a_i}{2^{i-1}R}\right]$$

$a_i = 1$ or 0

Fig2.2 Binary weighted resister ladder DAC

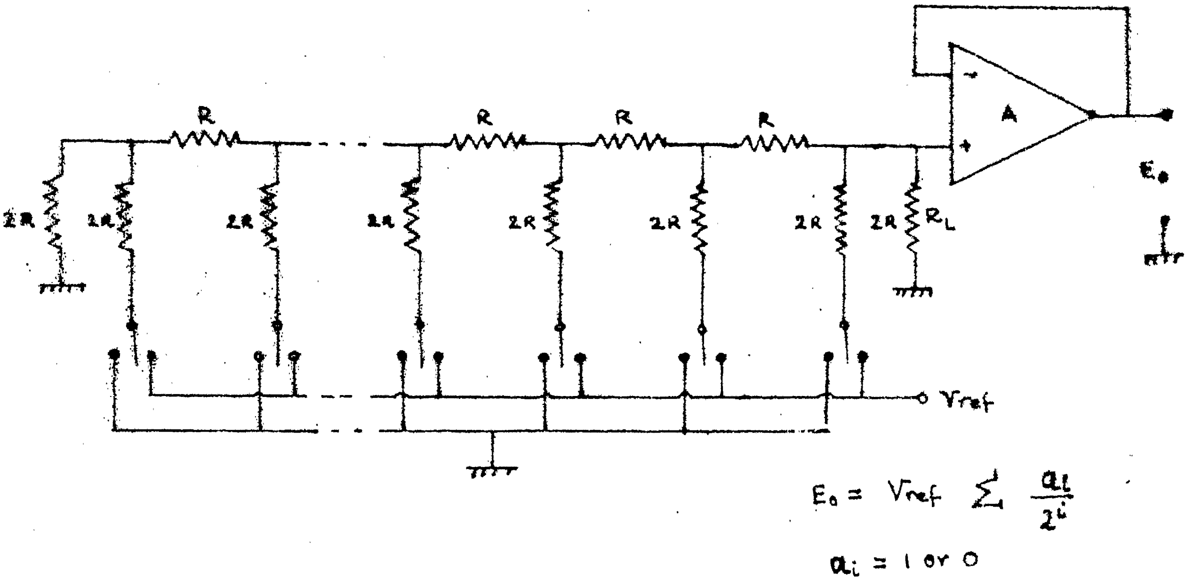


Fig 2.3 R-2R ladder DAC circuit

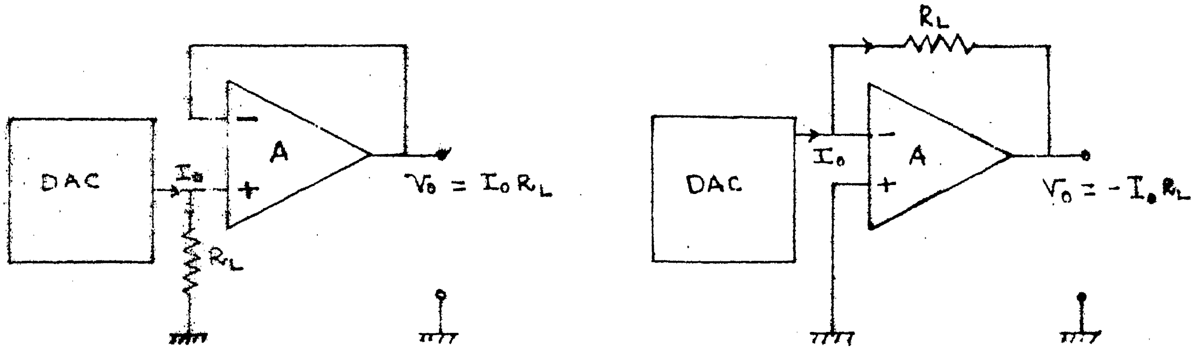


Fig 2.4 Output modes for current output DACs

2.2.1 Some Important Definitions

(a) Resolution : It is the smallest change in voltage (or current) output that may be produced and is the change that is caused by the LSB. It is given by $V_{FS}/2^n$, where V_{FS} = full scale voltage, n = no. of bits.

(b) Offset Voltage : It is the output voltage of the converter when the digital input is equal to zero.

(c) Differential Linearity Error : When the binary input changes by one bit, the output voltage should change by 'one LSB-change'. The converter's DLE is the magnitude of the maximum difference between each output step of the converter and the ideal step size of one LSB.

(d) Integral Linearity Error (linearity error) : This is the sum of the differential linearity errors for inputs up through the given input.

(e) Monotonicity : As the input code to a DAC is increased the output should increase and then the DAC is said to exhibit monotonicity. This is an important property of any DAC. In a non monotonic DAC, the output may decrease say from 3/16 to 1/8 as the input changes from 001 to 010, and in a control system this behavior represents an unwarrented phase shift of 180°, leading to instability.

(f) Absolute Accuracy : (inaccuracy) is the worst-case difference between actual converter output and ideal converter output.

(g) Relative accuracy : (inaccuracy) is the worst-case difference between actual converter output and ideal converter output after gain and offset errors have been removed.

(h) Glitch : When binary input changes, it establishes minor and major transitions. The most major transition is at the half scale (e.g. for 4 bit code the change 0111-1000). It may so happen (generally) that the switches act faster on a on-off transition than on an off-on transition and for a short time the DAC will have a zero output - (0111 - 0000 - 1000) and then the MSB is made 1. This large transient spike is called glitch. This is dependent on the logic delays of the circuitry.

(i) Settling time : This is the time taken for the DAC output to settle down to the voltage corresponding to the input code after the change (usually to a value within an equivalent of $\pm \frac{1}{2}$ LSB).

2.2.2 08 BC/0800 DAC

It is an 8-bit, current output, multiplying DAC.

It contains R-2R ladder, electronic switches, Current source and a reference amplifier.

The internal block diagram and the pinouts are shown in Figs. 2.5 and 2.6. The two current outputs are I_o and $\overline{I}_o$. I_o will rise from zero to full scale when input increases from 00 to FF and $\overline{I}_o$ will drop from full scale to zero as the input changes from 00 to FF .

Features

85 nSec Settling time

-10 to + 18V compliance

$\pm$ 4.5 to $\pm$ 18 V Supply

1 or 2 quadrant multiplication

Low Cost.

$$I_{FS} = \frac{255}{256} I_{ref}. \qquad I_{ref} = \frac{V_{ref}}{R_{ref}} \qquad 2\text{mA (recommended))}$$

For unipolar, operation connect a 5 K (max) load resistor between 4 to ground and connect 2 to ground (refer to Fig. 2.6).

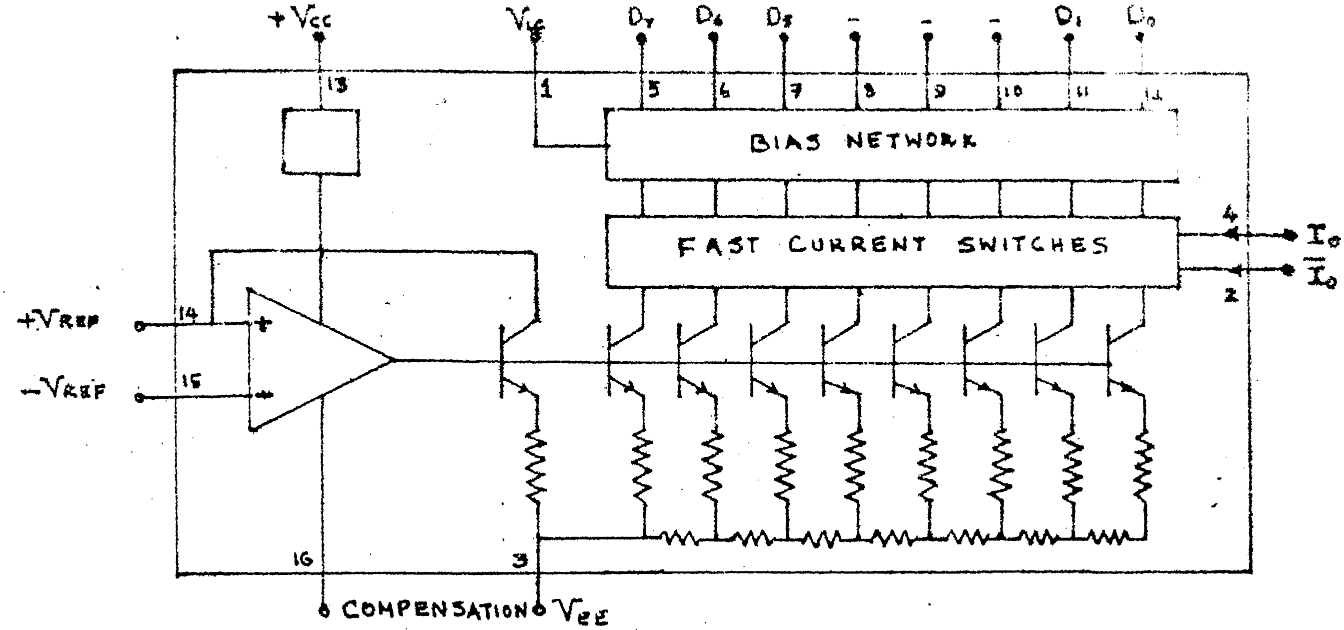


Fig 2·5 Internal blockdiagram of DAC-08

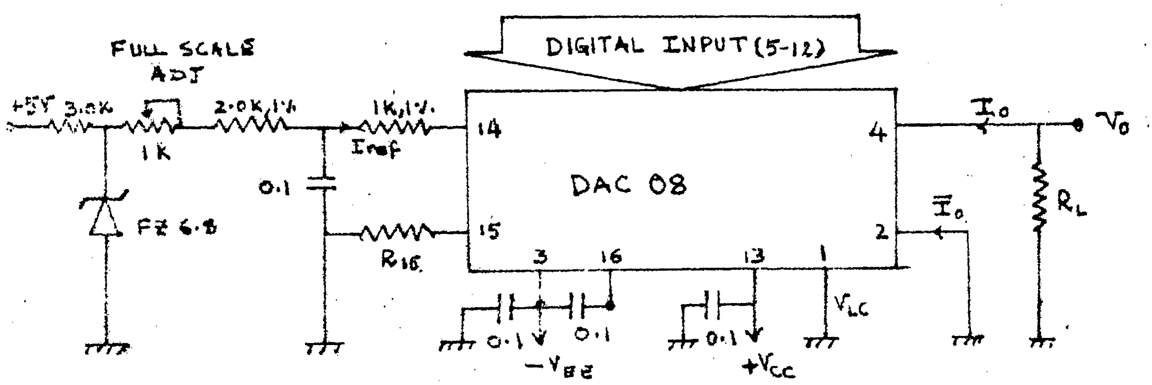


Fig 2·6 Circuit configuration for unipolar operation

2.2.3 Recent DAC Implementations

Recently the DACs have been built with the use of matched capacitors to realize the C-2C ladder and the weighted capacitor ladder. These are direct analogs of the resistor ladders. They are composed of MOS capacitors and switches and hence little current is drawn, and their power requirement is very low. Generally they are implemented on a chip along with other circuits (e.g. single chip μ c).

2.2.4 DAC Coding

For unipolar operation straight binary or BCD can be used. For bipolar operation offset binary coding is used generally.

1's and 2's complement coding can also be used.

2.2.5 Microprocessor Interfacing Considerations

Some DACs do not latch the input data and therefore require some external latches or PPI to hold the data constant over the required time interval.

An 8 bit converter can be interfaced with an 8 bit microcomputer easily, but if the number of bits is more than 8,

the data has to be properly latched with the help of inter-connected latches or ports (of PPI). However, all the bits have to be latched simultaneously by using double buffering. In our implementation the three 8-bit DACs are interfaced to the microcomputer through the 3 ports of PPI (8255A).

The ports of the PPI are programmed in Mode 0 - output mode. These ports are addressed as I/O ports in I/O mapped I/O.

2.3 ANALOG TO DIGITAL CONVERTER

We need to convert an anolog signal to a binary word before it can be given to a computer. The A/D converter takes an unknown analog signal (generally voltage) and gives an n-bit binary word representing the ratio of input voltage to the full scale voltage of the converter.

If V_{FS} is the full scale value for an n-bit converter then the voltage step required to produce one LSB change is given by $V_{FS}/2^n$ ideally. An n-bit converter can recognise 2^n steps from 0 to full scale input.

We encounter an unavoidable quantization error in ADCs because the output remains constant over an input range equal to one LSB (equivalent). That is for a given output

code the input can be anywhere within a one LSB quantization interval.

The ADCs have the linearity errors, (diffl. and intgl.) gain error, offset besides the quantization error. In addition, it may have missing codes, when the output never takes some of the codes at all (e.g. the output may jump from 101 to 111 and the code 110 is never attained).

The following chart gives various types of converters and their important characteristics. Their working principles are explained later.

Converter type	Conversion Rate at 12 bit resolution	Cost/complexity	Comments
1. Counter Ramp type	Low, upto 1000/sec	Low	-
2. Single slope	Low, upto 1000/sec	Low	Low speed at 12 bit lacks long term stability, conversion time variable.
3. Dual slope	Low, upto 1000/sec	Medium	Integrates input signal, can be used at high resolution - (20b) conversion time-variable.
4. Successive Approximation	Medium to high, upto 10^6/sec	Medium	10000 cps; upto 14-15b, needs stable input, conversion time fixed.
5 Flash (parallel)	Fastest 10^6 to 10^8/sec	High	Conversion time fixed.

2.3.1 Counter-Comparator Type ADC Circuits

The principle of working of the ADC can be easily understood with the help of the diagrams in Figs. 2.7 and 2.8.

It uses a n-bit DAC whose input is an n-bit binary (BCD) word from a counter.

The input voltage (under measurement) and the DAC output form the two inputs to the comparator. With the input V_{in} held constant, the counter is initiated and when the DAC output V_O just exceeds the input voltage V_{in}, the comparator gives a pulse which is used to inhibit the counting. The count registered in the counter corresponds to the binary output word of ADC.

Limitations : For longer bit lengths, 2^N may be too long and hence may slow down the conversion. Comparator settling time may cause some delay and introduce errors.

Advantage - Simple to implement.

2.3.2 Successive Approximation ADC Circuits

This is based on an intuitive technique that most nearly resembles the way we measure weights by trial and error.

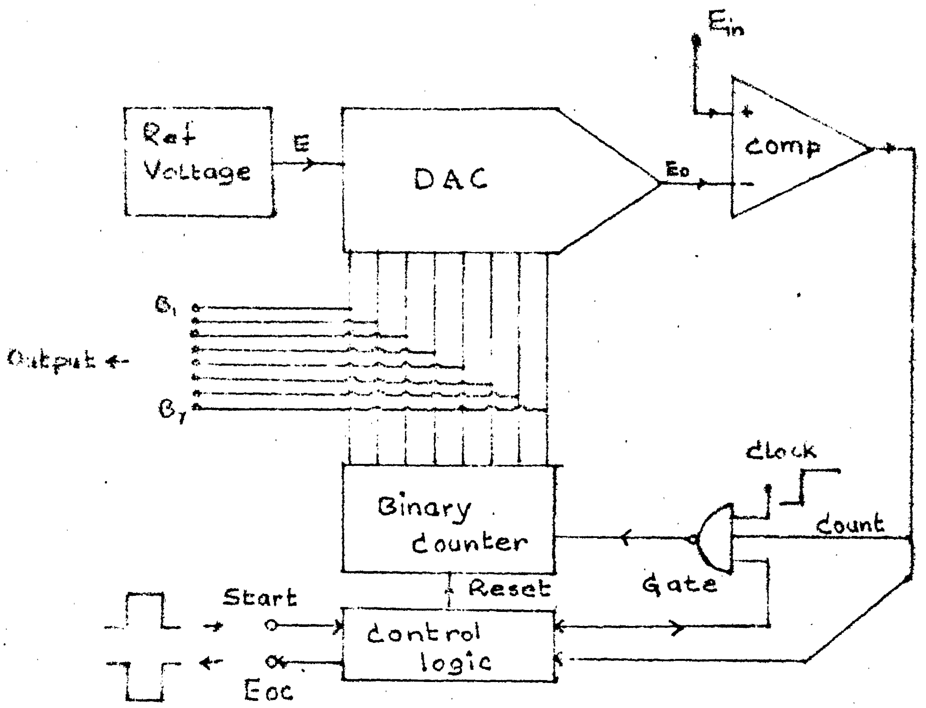


Fig 2.7 Counter Comparator type ADC circuit block diagram

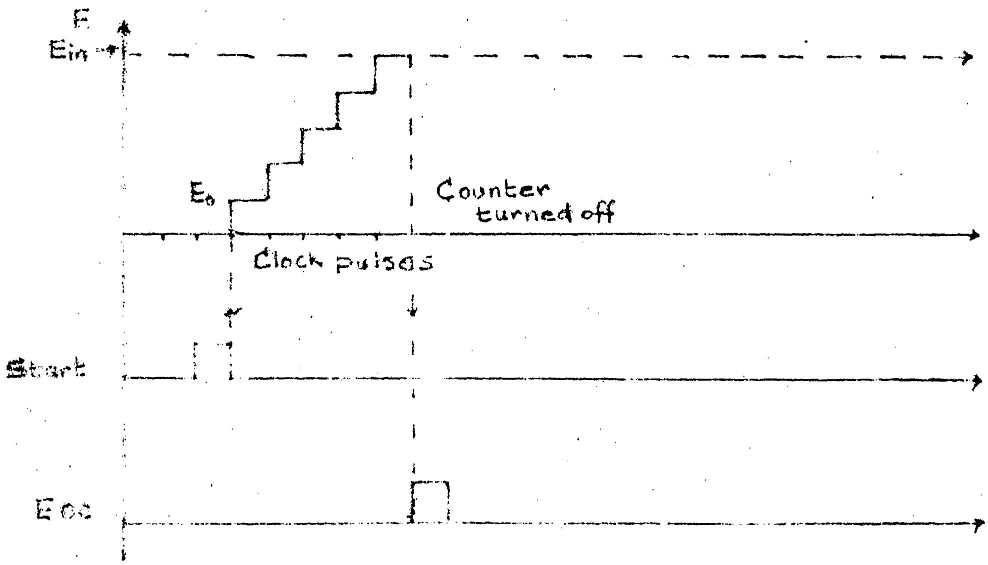


Fig 2.8 Timing diagram for the C-C type ADC

The tree diagram and the schematic block diagram illustrate the process more clearly (Figs. 2.9, 2.10). In the first step (say 3 bit converter) the input is compared with a DAC output at $\frac{1}{2}$ scale (100 input), if V_{in} V_{DAC} the DAC output is increased to $\frac{3}{4}$ scale (by changing DAC input to 110) and the process is continued till the end. If V_{in} V_{DAC} the DAC output is reduced to $\frac{1}{4}$ scale and the process is continued. That is, at each step the next MSB is evaluated till the LSB. (See the tree diagram).

2.3.3 Parallel or Flash ADC Circuit

It consists of a stack of 2^n-1 voltage comparators. One input of each comparator is the unknown voltage and the other is a reference voltage whose level is different for different comparators. These reference voltage levels are obtained from a simple resistor potential divider and a voltage reference. From Fig. 2.11, it is clear that the comparator output goes high when the input voltage is higher than the respective reference voltage. These comparator output levels are decoded to get the output binary word.

Salient Features

Very fast and the output is almost instantaneously obtained.

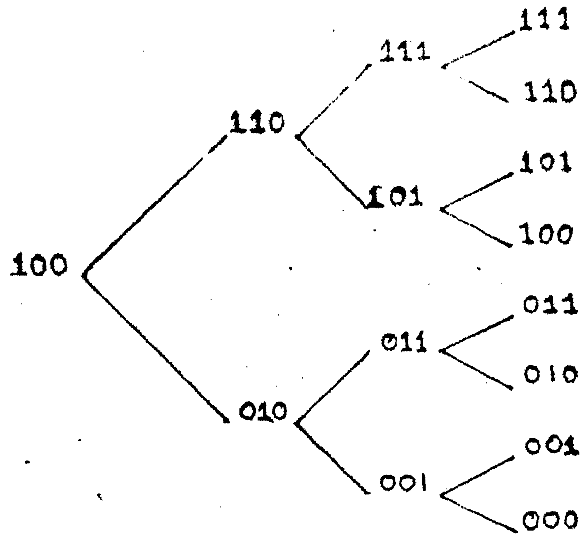


Fig 2·9 Successive approximation technique

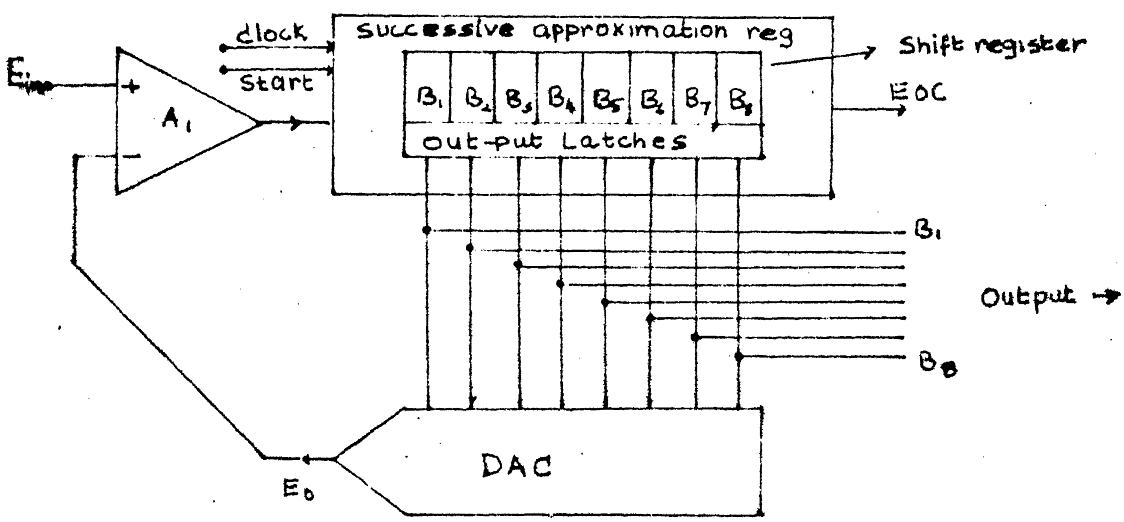


Fig 2·10 S·A ADC circuit block diagram

The number of comparators becomes large with increase in number of bits (2^n-1), and the decoder becomes complex.

The number of bits cannot be increased indefinitely, because the LSB equivalent voltage will be too small for the real voltage comparators.

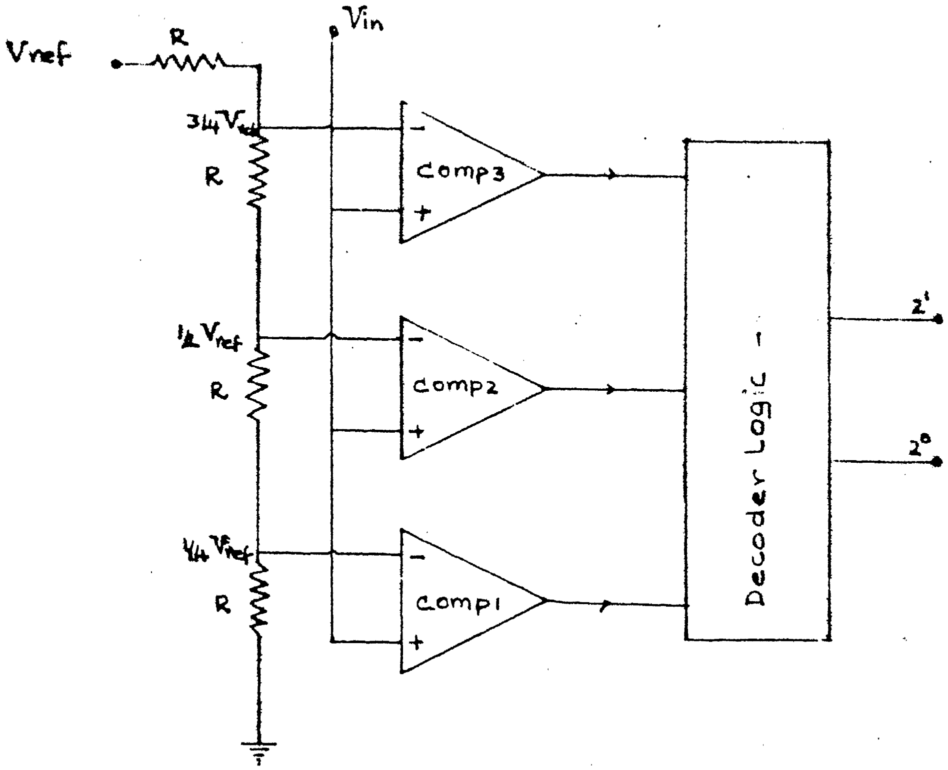
The circuit schematic and the decoding table are given in Fig. 2.11.

2.3.4 Integration ADC Circuits

Here the analog input voltage and the reference voltage or the input voltage alone is integrated using an analog integrator to get ramp signals. The operations are explained with the help of Fig. 2.12 and 2.13.

The Dual Slope type is explained in the following few lines. Here the input is integrated over a constant period of time corresponding to 2^n counts of a n-bit counter. Then the charge on the integrator C_f is discharged at a constant rate proportional to V_{ref}. When it is fully discharged the count registered in the counter gives the output binary word.

The block schematic and the timing diagrams are shown in Figs. 2.12 and 2.13.



Decoder logic table.

Input	C_1	C_2	C_3	Output 2^1	2^0
$0 - \frac{V_{ref}}{4}$	0	0	0	0	0
$\frac{V_{ref}}{4} - \frac{V_{ref}}{2}$	1	0	0	0	1
$\frac{V_{ref}}{2} - \frac{3}{4}V_r$	1	1	0	1	0
$\frac{3V_{ref}}{4} - V_{ref}$	1	1	1	1	1

Fig 2.11 Flash or parallel type ADC circuit

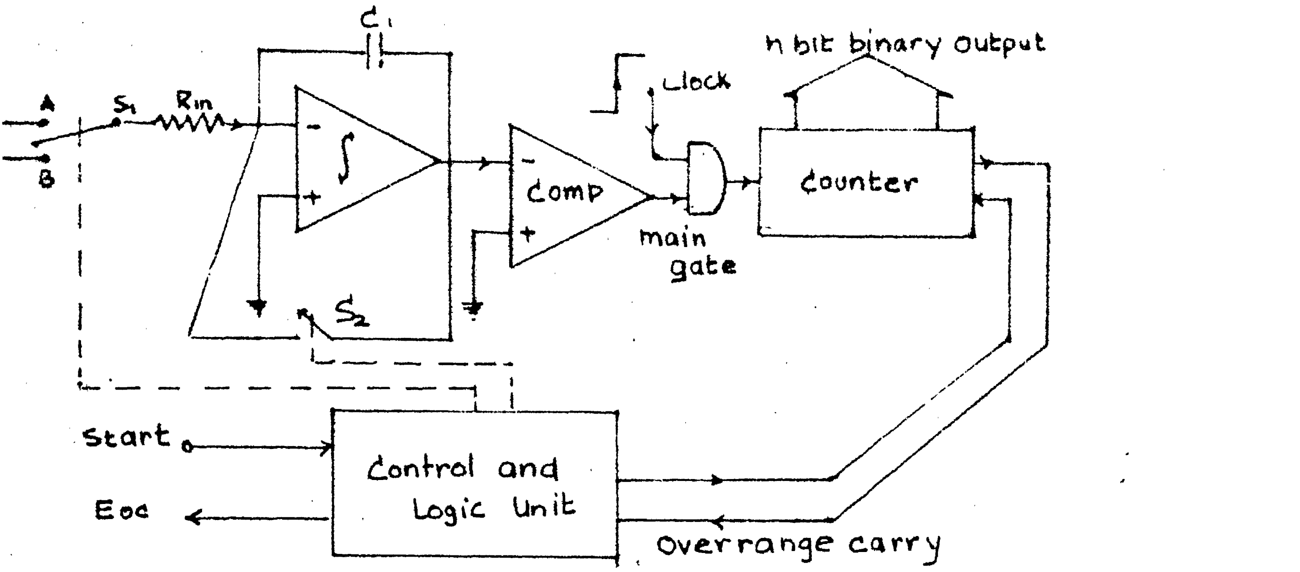


Fig 2.12 Dual slope integrator ADC blockdiagram

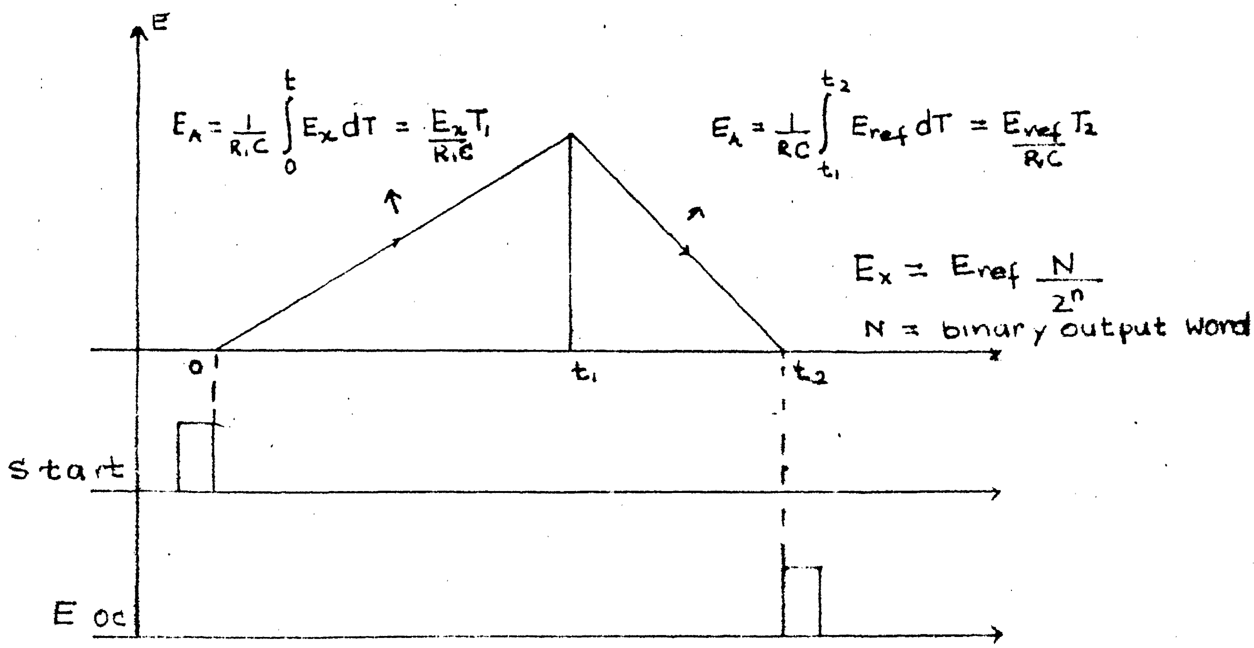


Fig 2.13 Timing diagram for dual slope ADC

2.3.5 EK 12B Integration Type ADC

EK 12B is an integrating type 12 bit A/D converter. It uses CMOS technology and is fabricated on a single monolithic chip. The schematic diagram and the associated external circuitry are shown in Figs. 2.14 and 2.15.

The working principle of an integration type A/D convertor is explained with the help of schematic diagram and timing diagram in preceeding article.

Features

Monolithic CMOS

Binary Coding - straight and offset option for unipolar and bipolar mode respectively

20 mW power consumption

12 bit accuracy

No missing code

Low cost

Conversion - time 1.8 to 24 millisec.

The analog input voltage range is programmable by means of external resistor by setting the current.

Standard operation is unipolar, but bipolar operation is possible by using external opamp to provide offset current from the reference.

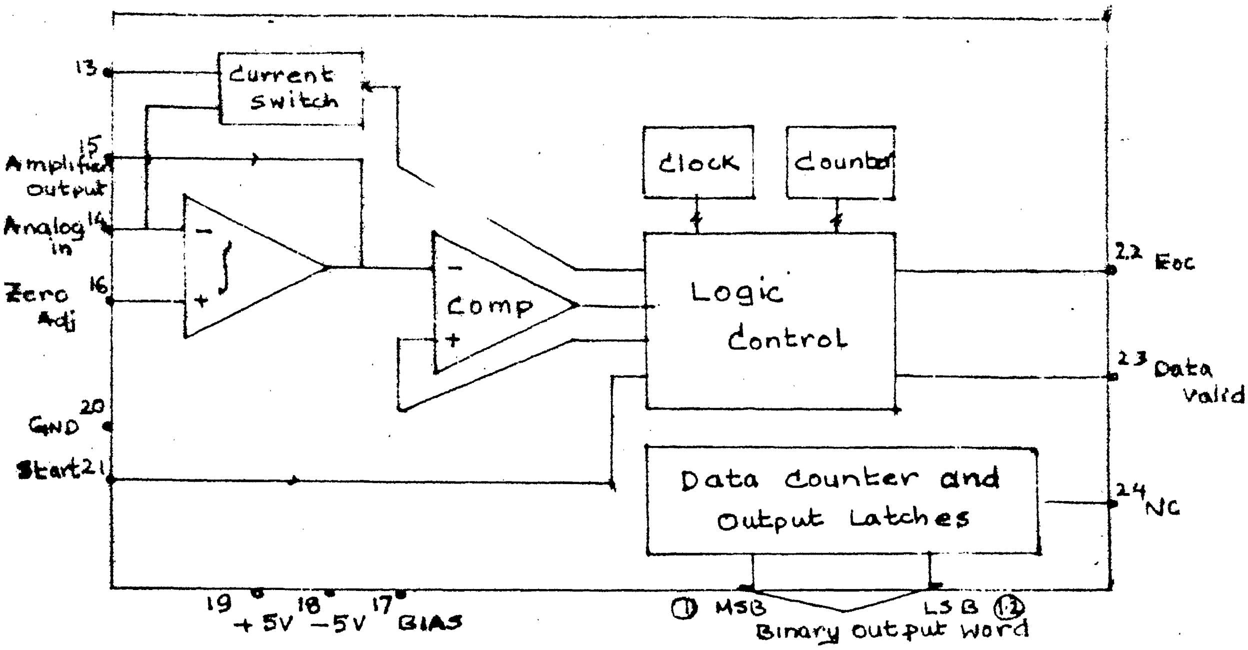


Fig 2·14 Block diagram of EK 12B ADC

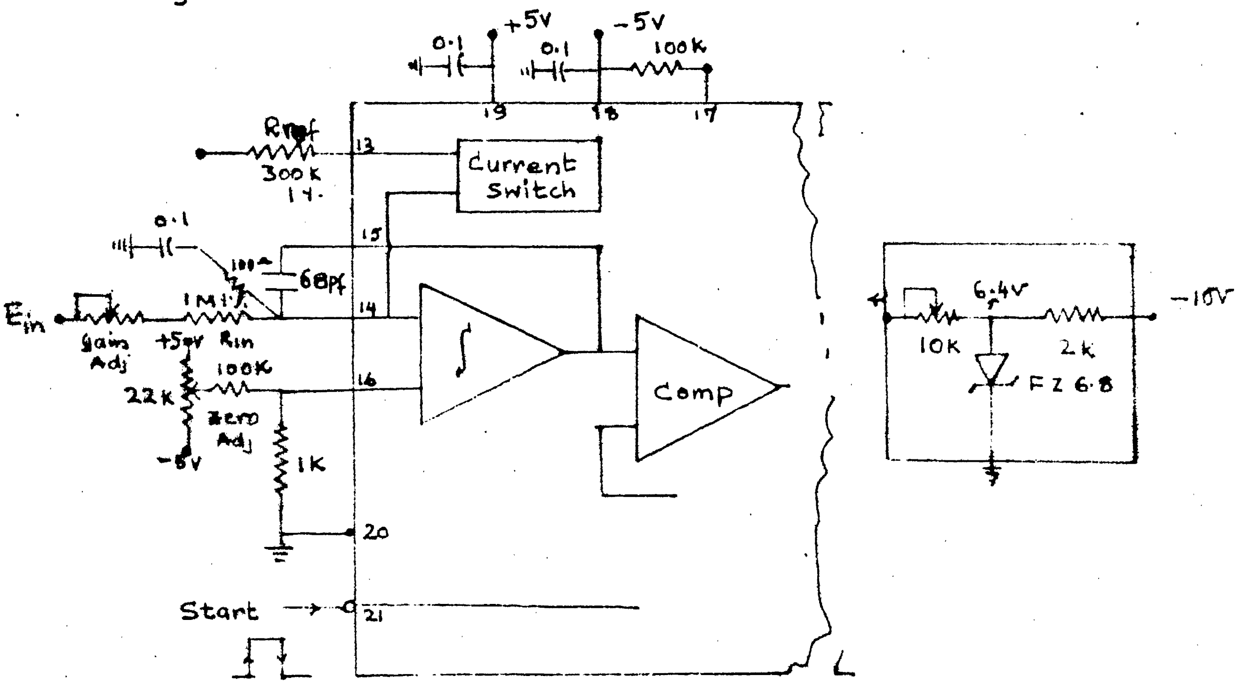


Fig 2·15 External circuitry for unipolar operation.

Power requirement is $\pm$ 5V D.C. at 2 mA giving a power consumption of 20 mW. The units come in 24 pin DIP.

More detailed information on this chip is available in many Datel Data acquisition system handbooks.

2.4 SAMPLE AND HOLD AMPLIFIERS

It is found that some ADC circuits such as successive approximation and integration type require that the input voltage be held constant during the conversion cycle. A Sample and Hold precisely does this by capturing the input signal at the instant the command signal is applied and by holding it constant over a time interval that is sufficient for conversion.

The basic circuit and principle of working are made clear with the aid of **Figs. 2.16a and 2.16b.**

The choice of hold capacitor (C_h) is critical. If C_h is large then switching errors is minimised but the performance is affected. Charge-up time depends on the time constant R_sC_h, R_s being the source resistance. And, if C_h is large the charge up time will be long.

An important specification of any S/H circuit is the droop-rate expressed as Volts/Sec. This is the loss of charge that the C_h suffers during the hold interval.

The acquisition time T_{AC} is the time required for the output to become equal to its input.

The aperture time T_{AP} - is the small amount of time required for the circuit to switch to hold mode. A good S/H should have T_{AP} not exceeding 50 ns.

Typical S/H errors and delays

T_{AC}	10 µs
T_{AP}	100 ns
OFFSET	5 mV
GAIN ERROR	0.05%
DROOP RATE	50 µV/mS.

2.4.1 <u>LM 398 S/H Amplifier</u> (National Semiconductor)

(SHM LM2 - DATEL-INTERSIL)

It is a low cost monolithic sample and hold circuit. Its salient features are high dc accuracy, fast acquisition, low droop rate. It operates as unity gain follower.

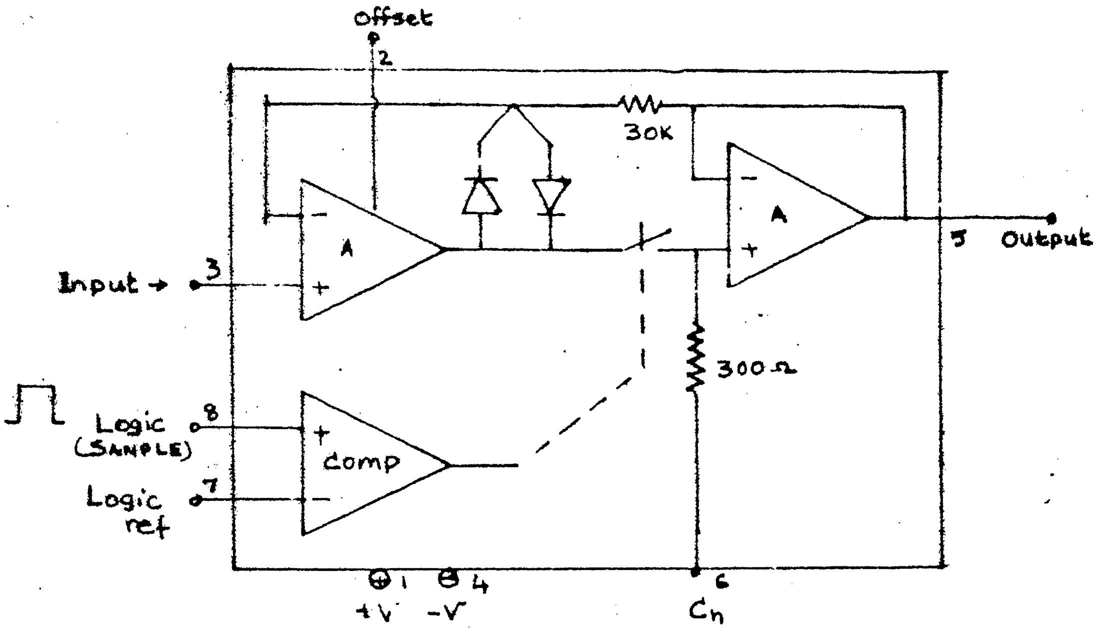


Fig 2.16 Internal block diagram of SAMPLE-AND-HOLD

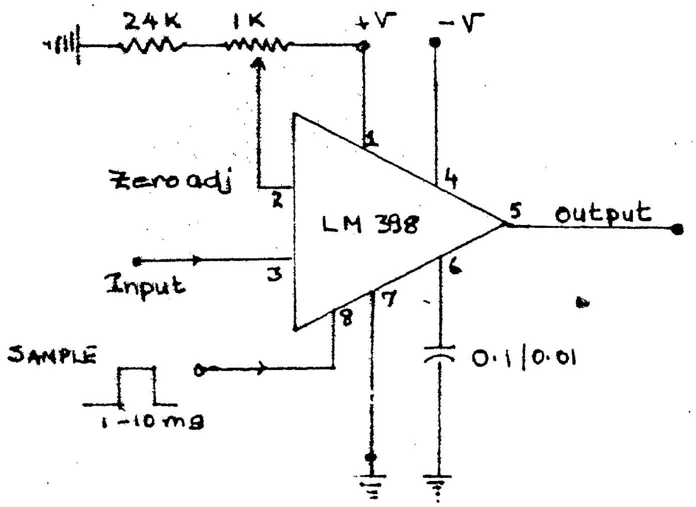


Fig 2.16a Associated circuitry

FEATURES

Acquisition time = 6 μsc

Input impedance = 10^{16} ohms

Drooprate 5mV/min with 1 μF hold capacitor.

180 mV/min with 0.1 μF hold capacitor.

Supply ± 5V to ± 18 V d.c.

TTL, CMOS compatible

gain error 0.002%

wide bandwidth

C_h = 0.01, R_L = 10K, Logic reference 0 - 2.5 V.

Hold capacitor - must be preferably polystyrene or polypropylene. Mica-capacitors should not be used.

The functional block diagram and the associated circuitry for the operation are shown in Figs. 2.16 and 2.16a.

2.5 ANALOG MUX CIRCUIT

It is generally uneconomical to go for a seperate ADC, a seperate output device etc, for each channel in a data acquisition system and instead, we go for a multiplexed system.

An analog multiplexer is an electronic switching system that will connect one of the several channels to a single device at any particular instant. The channels are

selected by impressing the desired channel-select binary word to the multiplexer.

In general it is found economical to place the multiplexer before the S/H-ADC circuits. The multiplexer connects one input channel at a time to the S/H and the ADC then processes the held-data. This scheme avoids the use of seperate S/H amplifier for each channel.

In our application however, we have multiplexed the output of S/H amplifiers. The output of the MUX feeds the ADC. This is necessary because the data here is an 'one-time affair', so as to say the signals from the channels need be measured at the same instant.

2.6 PROGRAMMABLE TIMER (8253)

Intel 8253 is a programmable counter or timer capable of operating in 6 modes, the modes of operation being software programmable. It does not require any other external hardware for its working.

It is organized into 3 independent 8/16 bit counters with a max count rate of 2 MHz. There is one control register (8 bit) and one status register, which are used to

program the counter and read the status of the operation respectively.

The counters (chip) can be addressed as I/O or memory. In our case its counters and the control/status registers are addressed as I/O ports. The clock to the counters is derived from the system clock, after being divided by 2 using a JK.

The gate serves as a trigger to the counter and is used a as shown in figures. The modes are explained with the help of timing diagrams (see Appendix).

8253 Control Word

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BC

SC - Select Counter

SC1	SC0	
0	0	Select counter 0
0	1	Select counter 1
1	0	select counter 2
1	1	illegal

RL - Read/Load

RL1	RL0	
0	0	READ/WRITE
0	1	Read/Load LSByte only
1	0	Read/Load MSByte only
1	1	Read/Load LSByte and MSByte

M - Mode

M2	M1	M0	
0	0	0	Mode 0 - Interrupt on terminal count
0	0	1	Mode 1 - Programmable one shot
X	1	0	Mode 2 - Rate generator
X	1	1	Mode 3 - Square Wave generator
1	0	0	Mode 4 - Software triggered strobe
1	0	1	Mode 5 - Hardware triggered strobe

BCD - N - NO BCD
1 - BCD

2.7 PROGRAMMABLE PERIPHERAL INTERFACE (8255A)

It is a general purpose programmable I/O device designed for use with intel microcomputers. It is a 40 pin Dual in line package.

It provides upto three 8 bit bidirectional I/O ports A,B,C and functions in 3 modes of operation.

Port A and the upper portion of port C form group A. The port B and the lower portion of port C form the B group. The functional configurations of 8255A is programmed by user's software. Mode is selected by writing the control word in the control register.

The 8255A's registers (ports) and the control word are addressed either as I/O or memory depending on the choice. In our implementation. 8255A ports are addressed as I/O ports. The chip select signal is generated with the help of a decoder using IO/$\overline{M}$ and a few address bits. The A_0 and A_1 qualify the addresses of individual ports.

A detailed information on 8255A is given in the Appendix.

In our implementation the 8255s are used in mode-0 (Simple output/input). It does not employ any handshaking in this mode. The mode word is first written into the 8255A control register. The data is either read from and written into the port depending on whether it is an input or output port respectively.

8255A (1) is used in mode-0 output. The ports A, B and C serve to interface the three 8 bit DACs. It is mentioned already that the DAC 08 does not have internal latches and hence the data has to be maintained by external latches and hence 8255 ports are used. Whenever the port addresses are chosen in a microcomputer based system care should be exercised so as not to clash with the existing port addresses. The addresses used are 70(A), 71(B), 72(C) and 73 for the control word. 8255 (2) is used partly in mode-0 output and partly in mode-0 input. Part A and Port C operate in input mode, interfacing the 12 bit ADC to the microcomputer (higher order 4 bits of Port A are 'dont care' bits). Port B operates in output mode, and is used for selecting the channels of the multiplexer.

2.8 SEMICONDUCTOR MEMORIES

The memory of a microcomputer system can be divided into two types namely, Data memory and program memory.

The program memory contains the programs, look-up tables (if any) etc, which in general are to be stored permanently and hence is worth storing on a non volatile or permanent memory.

The data memory generally consists of the test data acquired upon execution of some programs on the system. These data may be output through some interface to the outside world. They may be printed out or displayed on CRO as is needed. These information need only be stored temporarily on the system memory and hence are stored in RAM.

There are basically 3 types of non-volatile semiconductor memories namely, ROM, EPROM and E^2PROM. ROMs are programmed by the manufacturer and are not reprogrammable. In a system which is flexible and the changes are to be made more than once the ROMs are not the choice.

EPROM and E^2PROMs are extremely useful permanent-storage memories in a system such as ours. They are electrically programmable. EPROM is U.V. erasable and E^2PROM is electrically erasable.

EPROMs employ floating gate MOS technology. At normal operating voltages the gate is entirely isolated from the rest of the circuitry. By applying a high enough voltage between the source and the drain, a negative charge can be established at the gate, thereby putting the transistor in the conducting state. For erasing, the chip is exposed to UV light which drains this

negative charge and thereby erasing the memory. On complete erasure the whole unit is filled with 1's i.e. FFs.

Before reprogramming, it is in most cases advisible to erase the whole memory, even though it can be selectively programmed or over-written. (it must be recognised that while selectively programming, only those bits which are high can be made low and not vice versa).

The description of 2732A is given briefly and the detailed information is presented in the Appendix.

2.8.1 Intel 2732A

2732A is 4K byte, ultraviolet erasable and electrically programmable read only memory. It comes in a 24 pin DIP.

Its access time is 250 ns and is compatible with high performance microprocessors, such as the 8mHz-8086 and allows the microprocessor to operate without wait states.

The $\overline{OE}$ (output enable) control eliminates bus contention in multiple bus microprocessor systems. The 2732A has a standby mode which reduces the power dissipation without increasing access time. The maximum active current is 150 mA,

while maximum standby current is only 35 mA. The standby mode is achieved by applying a TTL high signal to $\overline{CE}$ output.

2732A is fabricated with high speed n-Ch MOS silicon gate technology.

2.9 MICROPROCESSOR

The design of digital system using microprocessor requires a different perspective from that using conventional digital logic. In the case of microprocessor based systems the hardware and software requirements are strongly related. Tasks are either performed in hardware or software and the decision is based on the trade-offs. The resulting systems performance depends greatly on the choice of hardware and software combination.

The system design with microcomputer involves the following basic stages.

1. Problem definition,
2. Evaluation of trade-offs,
3. Design of hardware and software,
4. Bread boarding of a prototype,
5. Testing of prototype,
6. Final modifications.

It is very important that the problem on hand be defined clearly by listing the requirements and then by arriving at a logical sequence of operations to be performed. Once the problem is defined in clear terms the characteristics of peripheral devices that link the microcomputer to the real world are defined, they are mainly the functional and timing relations. The amount of data handled is also estimated to decide the memory requirements.

After successfully completing the steps described above, we may proceed to evaluate the expediency of a microcomputer for our application. The following factors are of importance in evaluating its suitability, namely

1. word length (data)
2. Address length (size of the memory)
3. Numeric and logic capability (instruction set)
4. Interface requirements and existing support facility
5. Interrupt capability
6. DMA capability
7. Power and clock requirement
8. Cost ... etc.

The 8 bit microcomputers are found to be highly suitable for instrumentation and process control applications. Very rarely one goes for 16 bit or higher-bit microcomputers for such applications. The 8 bit microcomputers generally have 16 bit address which give them capability to have a maximum of 64K memory. A number of popular 8 bit microcomputers are on the market today . The manufacturers also provide a rich band of support devices to help designing the systems.

Among the popular 8 bit microprocessors are Intel's 8085/A, Motorola's M6800, Zilog Co's Z80, Fairchild's F8, NS's SC/MP etc.

Our choice of Intel 8085A is based on the following main considerations. The Intel microprocessor is supported with excellent hardware and software support facility and a rich documentation which is not found in the others listed above. Further the processor and the support facility are readily available at an economically feasible price.

2.10 MICROPROCESSOR WORKSTATION (8085/A)

A powerful and versatile 8085/A-based workstation has been developed at IITK EE Department and it was an obvious and judicious choice. Its salient features (Ref: Information

book-let prepared by EE department) are described in the following few pages.

The 8085A based workstation essentially consists of an 8085A based microprocessor kit with various interfaces for digital as well as analog input/output and a Video terminal-Keyboard interface for user interaction.

The system has two 8085A microprocessors, one of them is completely dedicated to handle the keyboard-video terminal interface and for displaying the information on the screen. This display processor has its own 2K byte RAM for storing the characters constituting a '24 (rows) x 80 (characters)' page displayed on the screen. The processor reads the characters from the Keyboard, sends them serially to the main 8085A through a RS232C link and displays the characters received from the main processor via the same serial link.

The main processor has associated with it a 16 K bytes EPROM (4x2732A) containing the Monitor, Editor, Assembler and the system routines. These EPROMS occupy the address space 0000-3FFF (Hex) in the memory map. The system has 8K bytes RAM (16x2114) occupying the address space 4000-5FFF. Addresses from 5800-5FFF are used for the stack and the scratch pad requirements of the system routines, and as such the addresses from 4000 to 57FF(Hex) are available to the users.

All the relevent pins of the microprocessor including the data bus and the demultiplexed address bus, have been buffered out at a 44 pin edge connector. Also brought out are the pins from an analog/digital input/output card (which has D/A, A/D converters, serial communication interface and PPIs) on the second 44 pin edge connector.

This workstation is developed to aid the user in developing software and hardware involved in a Microprocessor based system.

The Editor and the Assembler help the user to develop his assembly language software on the system. Also available is the EPROM programming facility to help the user store his debugged programme in EPROMS. The various assembler system routines that the system supports are explained in the chapter on software organisation.

The Fig. 2.17 shows the block schematic of the workstation. A small booklet is brought out by the EE Department to help in using the system.

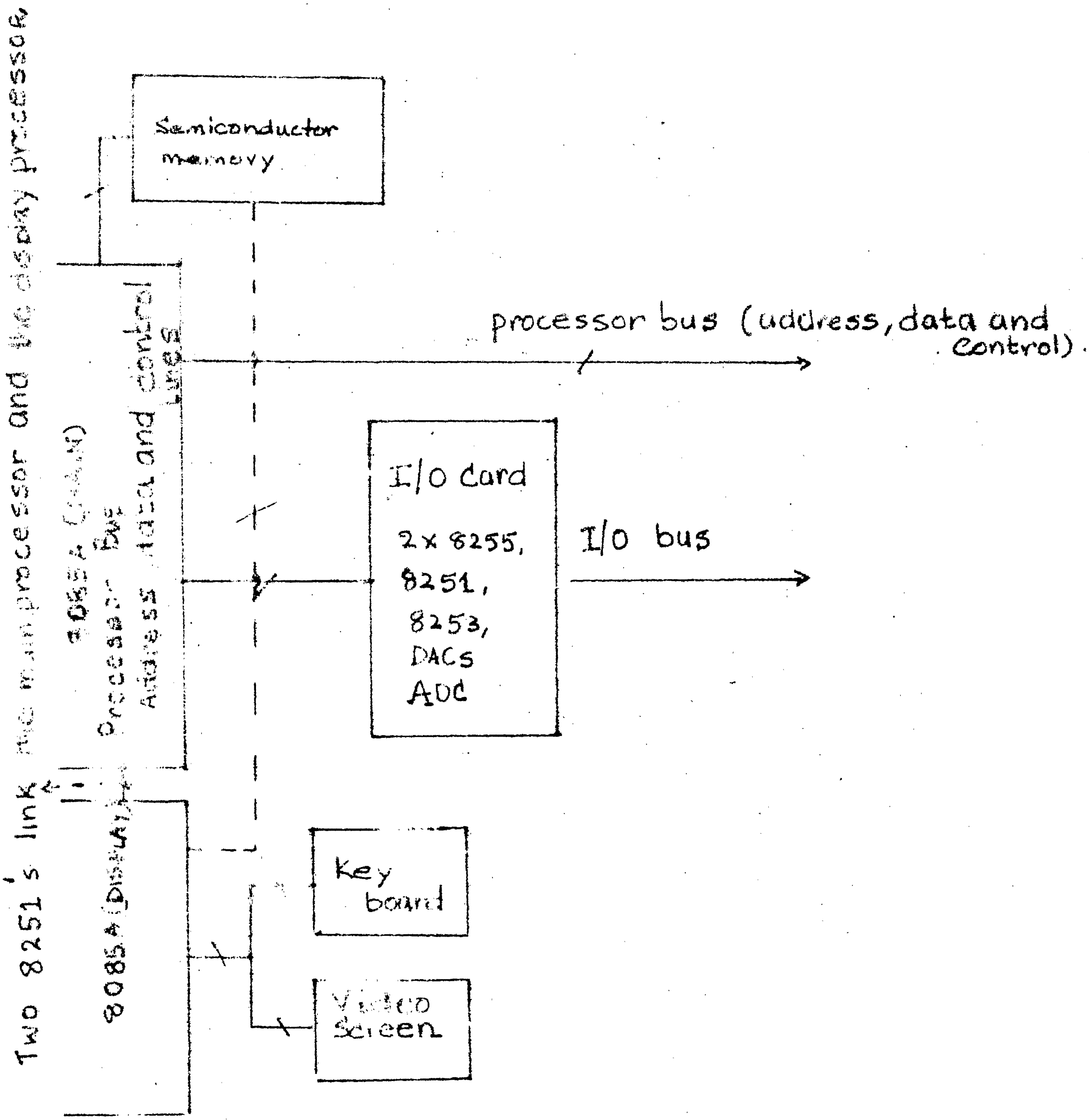


Fig 2.17 Block diagram of Workstation

CHAPTER 3

FUNCTIONAL MODULES AND SOFTWARE ORGANIZATION

3.1 INTRODUCTION

This chapter deals with the various functional modules that make up our system. The basic blocks that are required to build these modules have already been discussed in detail in chapter 2.

These modules are designed in such a way that they can be interfaced with any 8 bit microcomputer. They require a $\pm$ 12V d.c. dual power supply for their working. We firstly look at them individually, and, finally as an integrated unit.

3.2 DRIVER CIRCUIT

The PPI, D/A Converters, the summing amplifier, the current boosters constitute the 2-channel driver circuit. The schematic diagram of the circuit is shown in Fig.3.1.

The PPI ports A, B and C act as data latches for the inputs of DACs. The data is held constant till a new data is latched or until the control word is rewritten, in the later case the ports are all reset to 00. The ports and the control registers of the PPI are addressed as I/O ports in I/O mapped I/O.

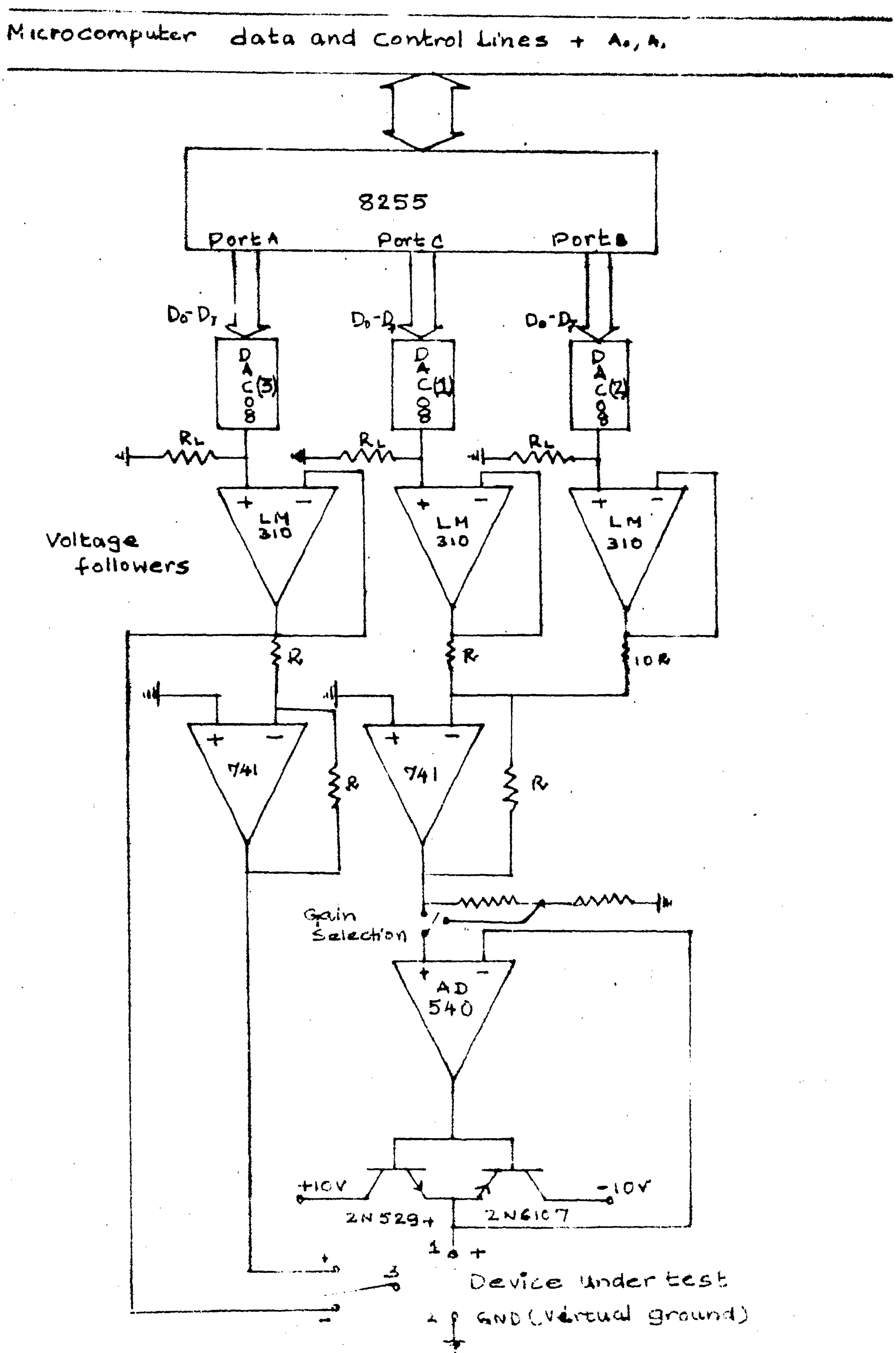


Fig 3.1 Two channel driver circuit

They are programmed as output ports (Mode 0).

The DACs and their associated circuitry are dealt with in detail in chapter 2.

The outputs of the DACs are buffered by means of opamp voltage followers.

The output of DAC(2) is divided by '10' and is summed with that of DAC(1) using a summing amplifier. This combination constitutes the channel 1 and the DAC(3) drives the channel-2.

The combination of DAC(1) and DAC(2) gives us two ranges of control over the output of channel 1, the main channel. The DAC(2) gives us a fine variation and the DAC(1) a coarse variation. This facility is extremely useful because the PN junction (non linear) devices have a highly sensitive region and a less sensitive region in their characteristics. (the ratio of change in current to change in voltage is a measure of sensitivity). The variation or the step length is selected by the software upon sensing the sensitivity of the region.

These DACs cannot drive more than 15-25 mA and hence these should be buffered further. The buffer circuit employed is a unity gain current booster which uses an opamp and a push-

pull amplifier. The push-pull stage employs a matched pair power transistors, and it can provide up to a maximum of 3 Amps drive in either directions.

The channel 1 drives the anode circuit of the semi-conductor device and the channel 2 drives the control terminal, if present in the device.

The overall response of the driver circuit with regards to speed and offset has been quite satisfactory over the working range. It may however be noted that since we are making the measurements of only the final output of the driver circuit the offset of individual stages are not going to introduce errors.

Additional heat sinks may be provided for the power transistors if the current range is to exceed more than 1 Amp . Each stage is provided with offset nulling circuitry.

3.3 SENSOR CIRCUIT

The current to voltage converter, the S/H amplifiers, multiplexer, the ADC and the PPI form the multichannel sensor circuit.

The anode voltage, the control terminal voltage and the plate current are measured by the sensor circuit. Generally

the multichannel measuring circuits use a single ADC and a single S/H and the input to the S/H is the output of a MUX. But in our application a seperate S/H for current and voltage are used and both these signals are sampled simultaneously. The outputs of the 'Sample and Holds' are multiplexed before being fed to the ADC.

The current-to-voltage converter has external gain settings for different type of devices. The software selects the appropriate range (gain) once the device code is entered. A switch is also operated to select the driving voltage in case of solar cell/solar module.

The S/H amplifiers are necessary because the ADC requires that its input voltage be held constant during the conversion intervals. For better results, more samples may be taken and averaged.

The ADC used is explained in detail in chapter 2. The ADC is operated in unipolar mode.

The control word for the MUX is loaded through port B of PPI(2).

The 'SAMPLE' pulse and 'START-CONVERT' pulse are issued by a programmable counter 8253A, operating in mode 0,

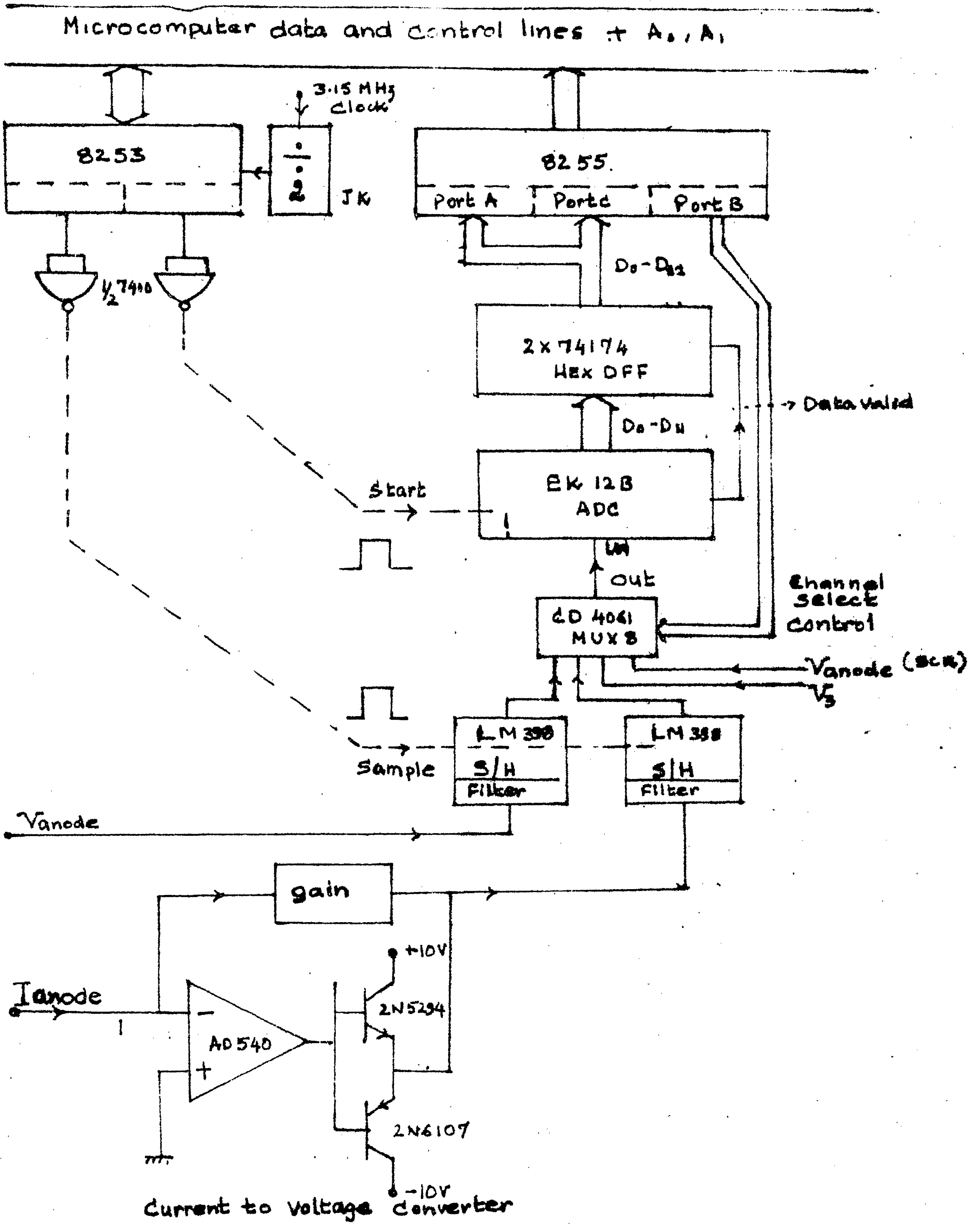


Fig 3.2 Multichannel sensor circuit

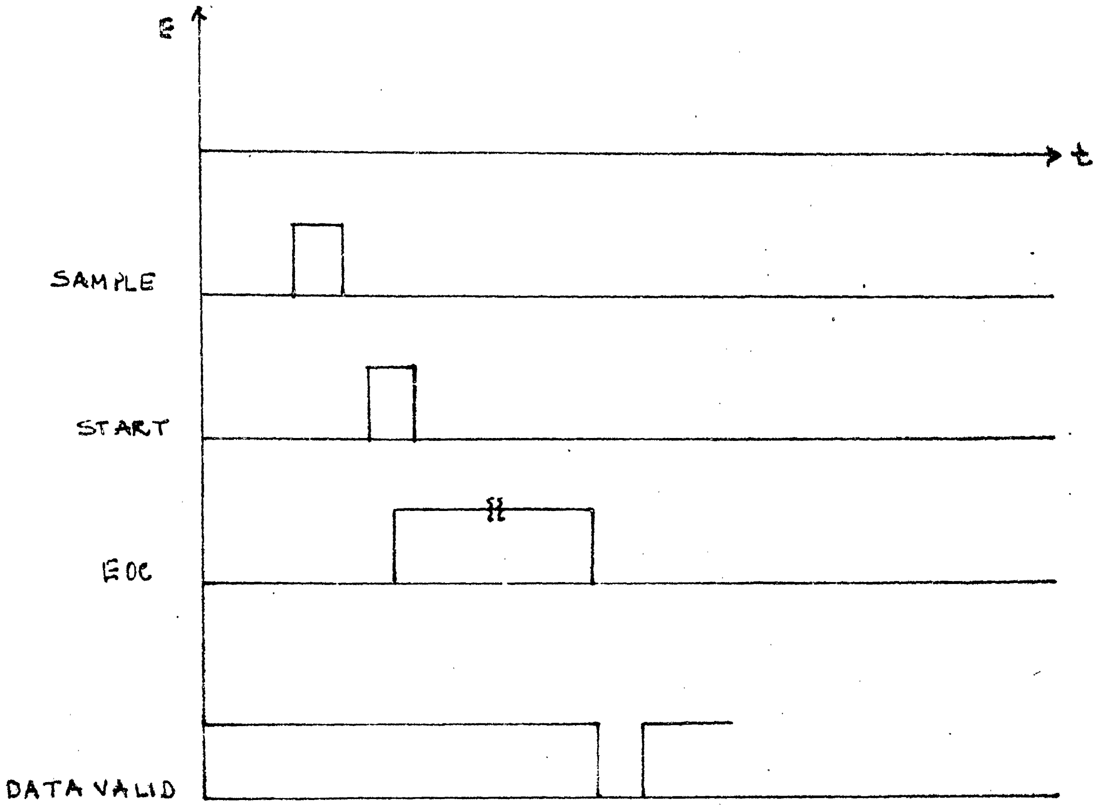


Fig 3·3 Timing diagram for the sensor circuit

with its gates pulled high. The width of these pulses is programmable.

The Data-Valid pulse of the ADC is used to latch the data of the ADC to a set of DFFs. which are later read by the microcomputer on polling the 'End of conversion' output.

The timing diagram and the circuit diagram for the sensor circuit are shown in Figs. 3.3 and 3.2 .

3.4 MEMORY BLOCK

The memory block in the system has an EPROM capacity of 8K bytes (2x2732A).

It has been already explained that 8085/A has 16 address lines and hence can address 2^{16} or 64 K bytes of memory (1K = 1024). The workstation's memory extends from 0000-6000 (Hex) comprising of EPROMS (16 K i.e 4 x 2732/A) and RAM (8 K, 16 x 2114). And, hence these locations (addresses) cannot be used by us. The user is allowed to use the memory locations C000(Hex) onwards for his EPROMS. Our 8K bytes start from memory locations E000, spanning the width E000-FFFF.

As already explained our system makes use of the RAM for data storage and manupulation.

Many of the system routines explained later are also used in the development of our software.

3.5 X-Y PLOTTER INTERFACE

The power of an instrumentation system or that of a testing facility lies in its ability to garner the data and to display it meaningfully. Some times it may be required that these results are recorded permanently for further study. The X-Y plotter is one such very popular equipment used to record the data in the form of characteristic plots. Many important inferences can be drawn from these plots on the nature of the behaviour of the device or system by looking at them and hence these records serve as extremely valuable information.

The X-Y plotter in our application is used to obtain the I-V characteristics. We employ on line recording. The characteristics are simultaneously plotted as the process of testing goes along. The X and Y inputs are taken from the outputs of S/H amplifiers directly and hence no additional interface circuitry is required.

If a separate interfacing circuitry, very similar to our drive circuit is employed, we can obtain the plots

after the necessary data is acquired. It should be kept in mind that even if we employ a separate interfacing circuitry there will not be any considerable improvement over the speed due to the inherently slow response speed of the plotter. The X-Y plotter is inherently a sluggish device due to the mechanical components that make up the driving system.

3.6 OVERALL SYSTEM

The three functional modules the driver, the sensor and the memory block are assembled on a single double sided Printed Circuit Board (Fig. 3.4). The memory block can be made separate, but it is found that the sensor and the driverneed be on the same board so as to avoid long connecting wires which introduce errors while handling low level signals.

The I-V characteristics of a device is obtained as follows. If the device is a three terminal one, the voltage used as the parameter is kept at the desired level and the other voltage is varied in descrete steps (for a two terminal device, however, this problem does not arise). Depending on the device and the characteristics being sought the sensitive and the less sensitive regions are recognised, and, accordingly

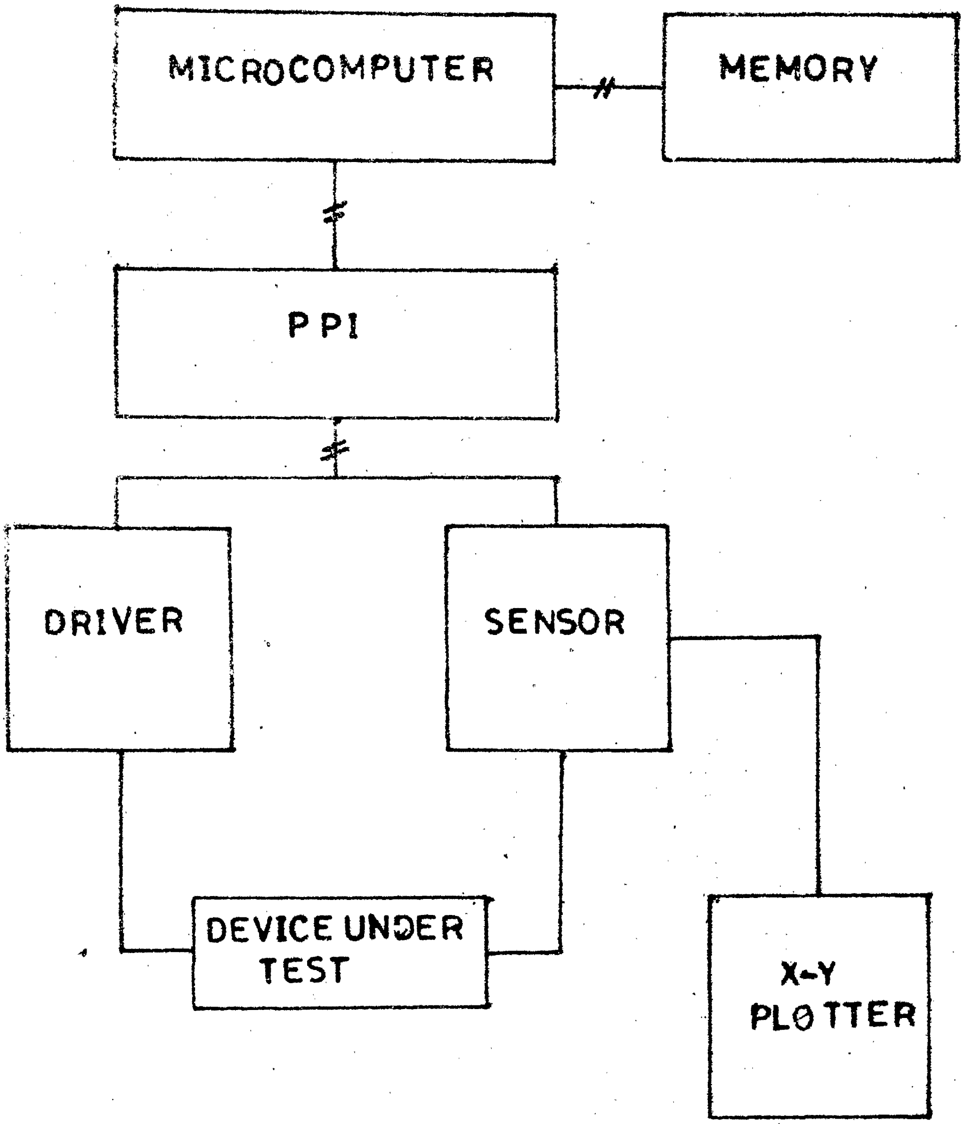


Fig 3.4 Basic System Block Diagram

the program applies the voltage steps. In the sensitive region the coarse control DAC is used. At each increment of the voltage, the voltage applied and the corresponding anode current is measured and recorded.

The device characteristics have some critical points which are taken care of by the program depending on the device code selected. The points corresponding to I_{SC}, V_{OC}, max power etc for solar cells, cut-in voltage for PN Junction diodes, breakover voltage for SCR etc are some examples of such points. Appropriate actions are taken at such points. The end point of the testing is sometimes left to the user's discretion, which is explained in greater detail in the chapter on testing.

The details of testing of different devices are given in the next chapter.

3.7 SOFTWARE ORGANIZATION

The software for our system is written in the assembly language of 8085/A. The software was developed and assembled on the microcomputer development system.

A master programming package named 'DEVICE' is proposed for testing of 2-3 terminal devices. It is aimed that

the package will be fully implemented and updated periodically. In our assignment this package is partly implemented, to cover a few 2-terminal and 3-terminal devices such as solar cells, PN Junction diodes, LEDs, Zener, SCR etc. The package is to be updated with test routines for other devices so as to create a master facility.

Our work can be treated as the foundation for the proposed. Computer aided device testing facility.

The software is implemented in highly modular fashion to aid in easy understanding and further modification. The entire task is broken up into smaller subtasks. The basic subtasks are accomplished by some first level (in the nest structure) subroutines. Various levels of nesting and the routines of these levels are explained in detail. The package also makes use of some of the important display routines and arithmetic routines that are provided by the system (workstation). These system routines and their functions are listed too in the following section.

Level 1

At this level, that is the innermost level we have the system routines and those routines which do not use any

other routine except the system routines. They are listed and explained in the following lines.

SYSTEM ROUTINES

Name	function	Affected registers
READ	Reads an ASCII character from the keyboard and stores it in accumulator	A
PRINT	Sends the ASCII character held in Accumulator to the screen	None
CRLF	Sends the ASCIIs for carriage return and line feed to the screen	None
TWOSP	Sends the ASC11 for blank twice to the screen	None
BIHEX	Sends the Hex number (XX) held in A to the screen	None
HLPNT	Prints the contents of HL as 4 Hex character and gives two blanks on the screen	None
PNTMS	Prints a string of characters stored from locations [BC] onwards until '*' is encountered	BC

Note : The level 1 routine may require some meaningful data to be stored in some memory for their satisfactory working and they may not be totally independent. Level 1 just means that they are at the inner most loop in a nested structure.

Name	Function	Affected Registers
DELAY	Generates a software delay given by Delay = 7.2 μsec * [BC] + 9 μsec	A,B,C
MULT	Multplies two unsigned binary numbers : [HL] = B * A	A,B, DE, HL
EMULT	Multiplies two 16 bit unsigned binary numbers : [DEHL] = [DE]* [BC]	ALL
BDIV	Divides a 32 bit unsigned number by a 16 bit unsigned number [HLBC] /DE HL Reminder BC	ALL
BTBCD	Converts a 16 bit binary number held HL to BCD and stores it in memory locations starting from [DE] (MSD first)	ALL
BCDTB	Converts a 4 digit BCD stored from location [DE] into 16 bit binary in HL	ALL
HV (1,2,3)	Applies the next higher input word to DAC1, DAC2, DAC respectively and stores the next count in the memory	A
LV (1,2,3)	Applies the next lower input word to DAC1, DAC2, DAC3 respectively and stores the next count in the memory	A
SAMPL	Applies the sample pulse to S/H amplifiers	A,B,C
START	Applies the start pulse to ADC	A,B,C
SLCT (1,2,3,4)	Selects the channels 1,2,3,4 of the mux	A

Name	Function	Affected Registers
STORE	Gets the ADC output into HL	HL
AVG	Computes the Average of four 16 bit numbers	A,HL,B,C,
LODNG	Stores the average counts of voltage and currents in consecutive location from an address stored at 5000 (Hex) and increments the addresses	HL, BC, A,
DISP	Displays a 4 digit BCD number on the screen. (XXXX)	ALL
DISP1 (1,2,3,4)	Displays 4 digit BCD number with a decimal point	ALL
INITN	Initialises 8255(1) and 8255(2) with proper control words. Initialises the DAC outputs to Zero. Programs the 8253A counter in Mode 0.	A
VXI1	Computes the product of v_{oc} and I_{sc} of solar cell	ALL
VXI	Computes the product V X I of solar cells	ALL
LMPVI	Stores the values of V and I at max power (solar cells)	A,B,C,H,L.
VXIP	Computes the value of $VI/V_{oc}I_{sc}$ at each step and stores the present highest value in the memory.	ALL
XEFF	Computes the efficiency of solar cell/solar modules	ALL
RCH	Computes V_{oc}/I_{sc}, the characteristic resistance of solar cell	ALL

Name	Function	Affected Registers
RSMAX	Computes the output impedance of solar cell	ALL
VICHT	After the test is over if this routine is called, it displays the V-I characteristics (values) in mV and mA respectively on the screen. It has no meaning if called independently though it may run.	ALL

Level 2

The subroutines at level 2 may refer to system routines and the routines on the level 1. They may not refer to the routines on level 2 or higher (all registers are affected).

LOAI : obtains the values of ADC counts corresponding to anode voltage, anode current and the control voltage (for 3 terminal device only).

VI4 : obtains 4 samples of V and I ADC counts and stores them in memory

V3 : obtains 4-samples of ADC counts corresponding to V3 (the control terminal voltage)

SHCKT : obtains the short circuit current of solar cell, stores it and displays it on the screen.

VOCKT : obtains the open circuit voltage of solar cell and stores it. It displays the open circuit voltage in mV. Firstly it increments the sensitive DAC, DAC2 and then DAC1 At each increment the current is sensed and when the current becomes zero the routine is exited.

CHECK : This routine checks whether the initialization has been done properly or not and if initialization is not proper, the INITN routine is repeatedly called until the initialization is proper.

VIMP : It stores the values of V and I counts at maximum power point and displays them on the screen.

Level 3

These routines can be executed independently and they generally perform a complete test or a part of the test. These may refer to the system routines and the routines in the lower levels. They may print some messages and instructions to the user who has to follow them correctly.

MEASR : It obtains 4 values of V and I ADC counts and obtains the average values of the counts and displays them on the screen. This may not be executed independently.

SOLAR : It obtains the V_{oc}, I_{sc} and V-I characteristics of a solar cell/panel at a fixed illumination. (Testing details explained in chapter 4).

RUNN : After obtaining V_{oc} and I_{sc}, the characteristic plots, the values of V and I are stored from location 4200 Hex onwards. The values are displayed for user's verification.
Here at each point 4 samples are taken and the average is stored.

TEST1 : It prints the values of V_{oc}, I_{sc}, R_{out}, Efficiency, FF of solar cell/module after the test is made (at a constant illumination)

FAST1 : It is similar to RUNN except that in this case the averaging is not carried out.

DIODE : It gets the forward V-I characteristics of a PN Junction diodes Zener, LED etc. It prints the cut-in voltage and after the cut-in voltage, the continuation of the test is left to the user's discretion.

Level 4

FULL : Gets the full V-I characteristics of solar cell under different illuminations. This gives a no. of prompt messages for the user and they have to be carefully followed. Here the voltages and current samples are averaged to get accurate results.

FAST 2 : Gets the V.I characteristic of solar cell/panels under different illuminations. The V and I values are not averaged. The values are stored and the results are also plotted.

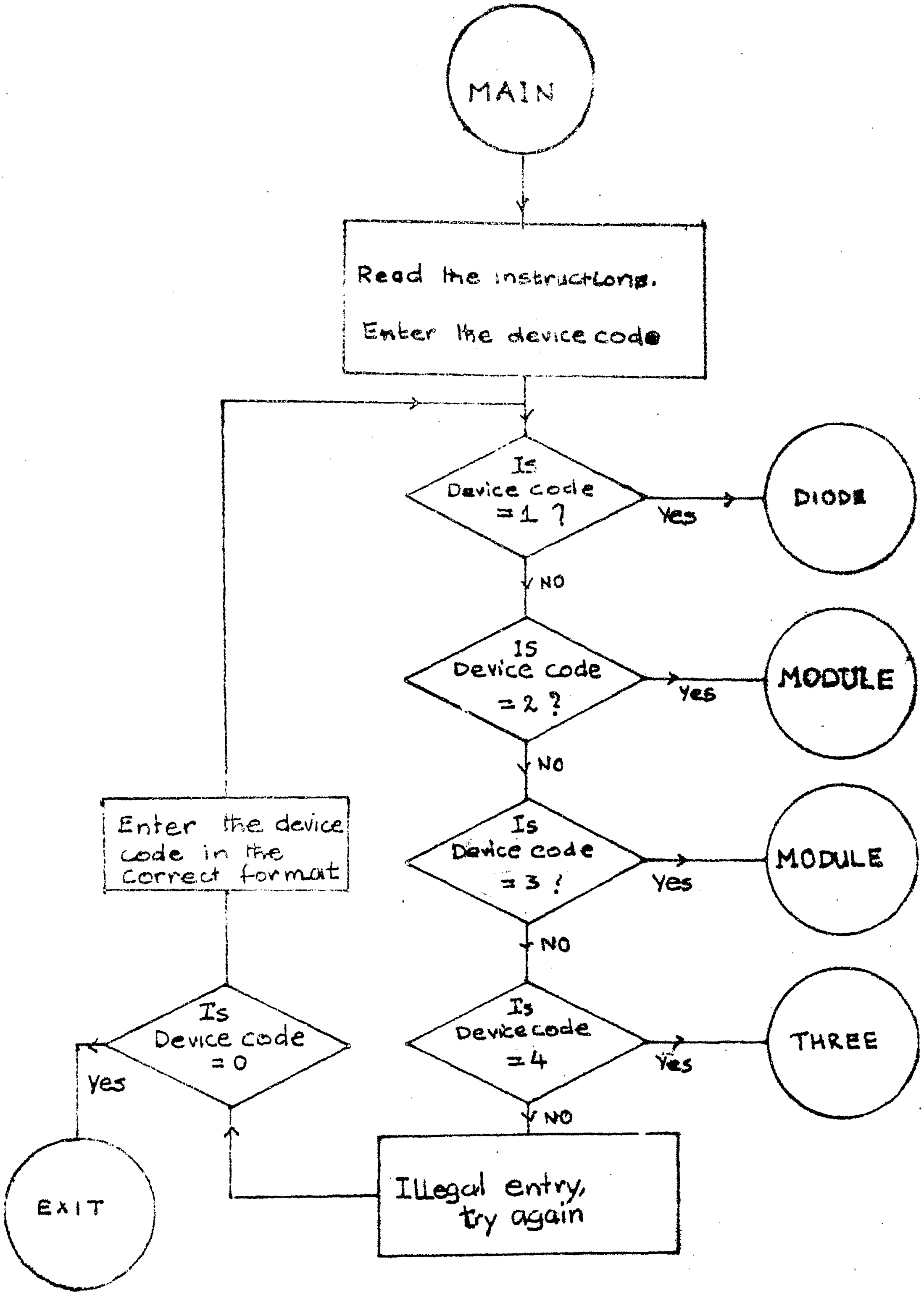
Module : Here the option for testing 'with-averaging' or testing 'without averaging' is made

Twice : Here the corresponding routine is selected for the three terminal device testing.

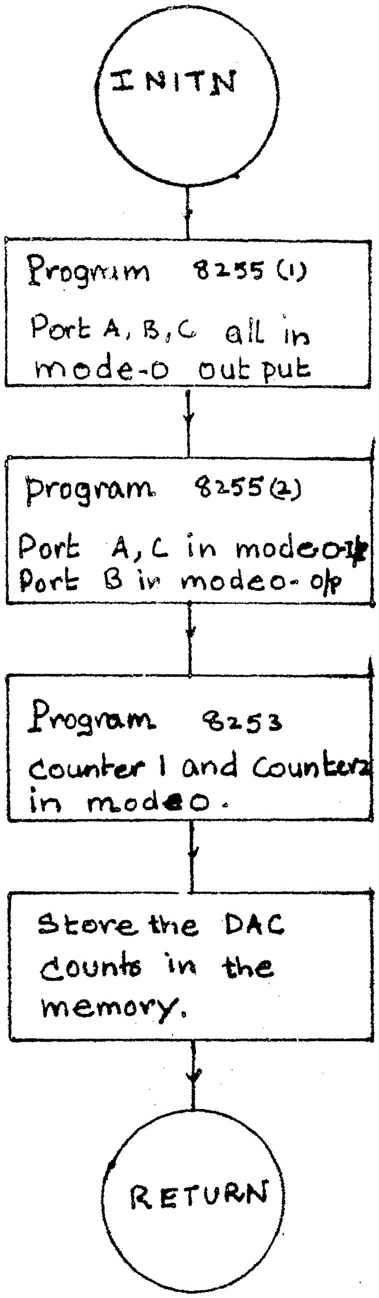
Level 5

MAIN : This is the main program and the following sequence of operations is executed.

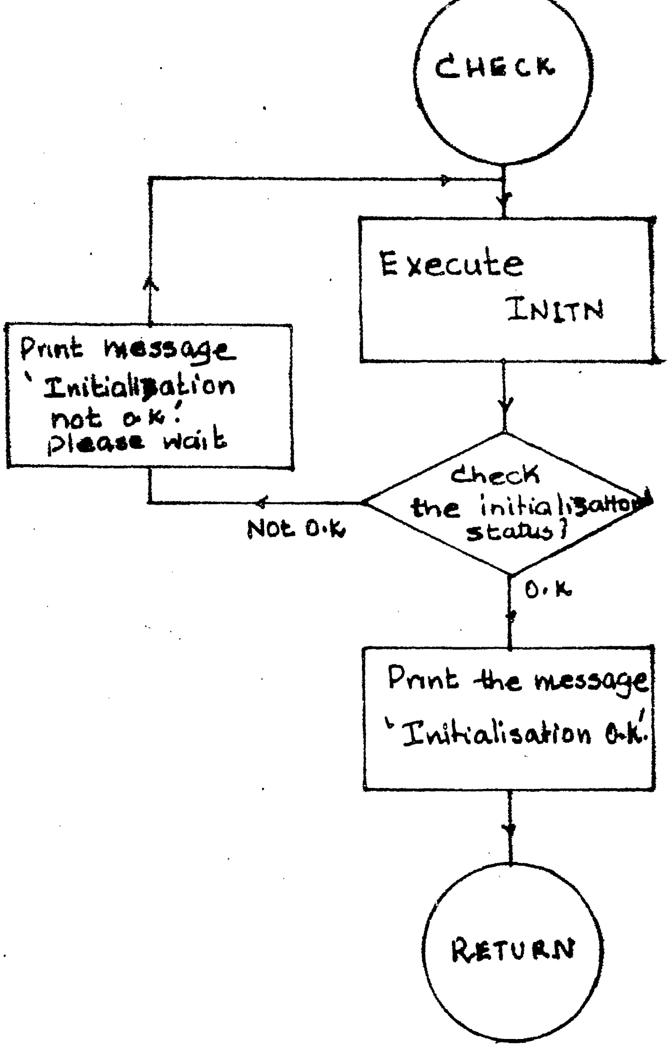
The instructions for using the system are displayed. Upon the action of the user, the system selects the program corresponding to the device code and carries out testing. This program is under the user's control and can be halted in any intermediate point and continued further.



Flowchart-1 MAIN



Flowchart-2 INITN



Flowchart-3 CHECK

CHAPTER 4

TESTS AND RESULTS

4.1 INTRODUCTION

In this chapter the procedures for testing of various types of devices are explained. In any device characteristics we encounter a highly sensitive and a less sensitive region . A more sensitive region is one in which there is a large change in current for a particular voltage change. For example the portion of solar cell characteristics near the open circuit, the portion of diode or SCR characteristics after the cut in or break over represent the sensitive regions. Saturation region of BJT, FET, the portion of V-I characteristics near short circuit of a solar cell etc. are examples of less sensitive regions. In the sensitive region the DAC(2) is used and in the less sensitive region the DAC(1) is used. Also the semiconductor characteristics exhibit some points (critical) at which there is some sudden change, for example, cut in voltage or breakover voltage of a diode or SCR. The above mentioned factors are important in arriving at the procedures for testing various types of devices.

4.2 SOLAR CELL CHARACTERIZATION

The solar cell can be regarded as an opto-electric transducer. Therefore it is of importance to study its be-

haviour under different illumination intensities.

The important parameters of a solar cell are V_{oc}, I_{sc}, max power, fillfactor, efficiency, R_{out} and R_{CH}. These parameters have to be determined under different illuminations or excitations. It is important to note that when a solar cell is employed as an energy source (power source), to get the optimum output the solar cell should be biased at a point of maximum power. And this has to be computed regularly during the day (as the intensity of sunlight is changing) and the bias should be properly maintained to get the best out of the installation.

FAST : This routine gets the values of V_{oc}, I_{sc} $(VI)_{max}$, V_m, I_m, R_{out} (R_s as high illumination), FF and efficiency and obtains a plot of V.I. The results are displayed on the screen on user's request. The routine is generally repeated for different illumination intensities. To obtain the efficiency the input light energy has to be entered through the keyboard. (in Milliwatts).

The following sequence of operations is performed during the execution of the routine.

Step 1 : **Initialize the system.** . Connect the device and the X-Y plotter to the terminals marked device and X-Y respectively .

Step 2 : Increment DAC(2) in steps and sense the current .

Step 3 : If the current = 0 or if the input to DAC(2) = FF then go to Step 6 or Step 4 respectively, or else go to step 2.

Step 4 : Increment DAC(1) in steps and sense the current.

Step 5 : If the current = 0 or if the input to DAC(1) = FF then go to Step 5 or Step 7 respectively or else go to step 4.

Step 6 : Now store the initial values of DAC counts for further testing as follows.

The DAC counts now registered (corresponding HV1, HV2) correspond to the V_{oc} condition. These counts are now stored as initial counts of LV1 and LV2 routines. For drawing the plot and getting the V and I values we go from V_{oc} to I_{sc} (V_{sc}).

Initially we decrement the input of DAC(2) the sensitive DAC to produce smaller voltage steps for the sensitive portion.

Once the input corresponding to DAC(2) is 00 the control is transferred to DAC(1).

Now the DAC(1)'s input is decremented till we get 00.

At each voltage variation the V, and I are measured and the product VxI is computed. The present value of VxI is compared with the previously stored 'max' value of VxI product. If the present value of VxI is greater than the previous one the present value is stored as VxI (max) and eventually at the end we will get the (VxI)max. Also stored are the V_m and I_m corresponding to the max (VxI) product, V_{oc} and I_{sc}.

$R_{CH} = V_{oc}/I_{sc}$ and

$R_{out} = (V_{oc} - V_{mp} / I_{mp})$ are computed. R_{out} gives us the output impedence of the solar cell at maximum power. It is verified that at high intensities $R_{out} \simeq R_{series}$.

The FF = $\frac{V_{mp}\ I_{mp}}{V_{oc}\ I_{sc}}$ x 100 is computed and stored.

The input watts is entered through the keyboard. (in watts/cm^2)

Input watts = intensity/x Area of the device over which the light is incident (in cm^2).

and the efficiency at max.power is computed as $\frac{V_{mp} \cdot I_{mp}}{\text{Input}}$ x 100.

All these parameters are displayed as shown in the photographs of the screen.

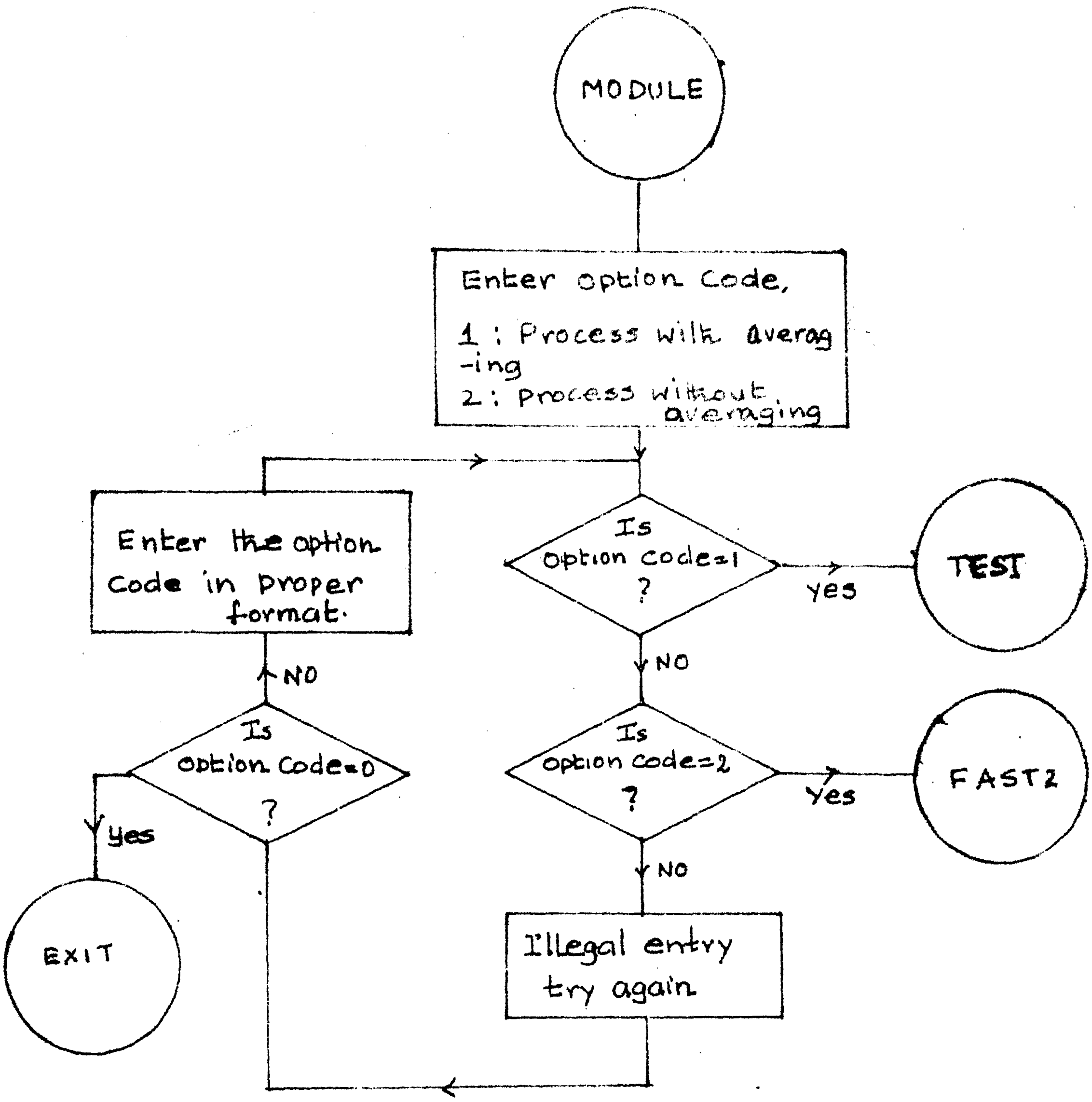
The corresponding plots for different illuminations are obtained on the graph paper.

The V-I values are displayed on the screen on user's command.

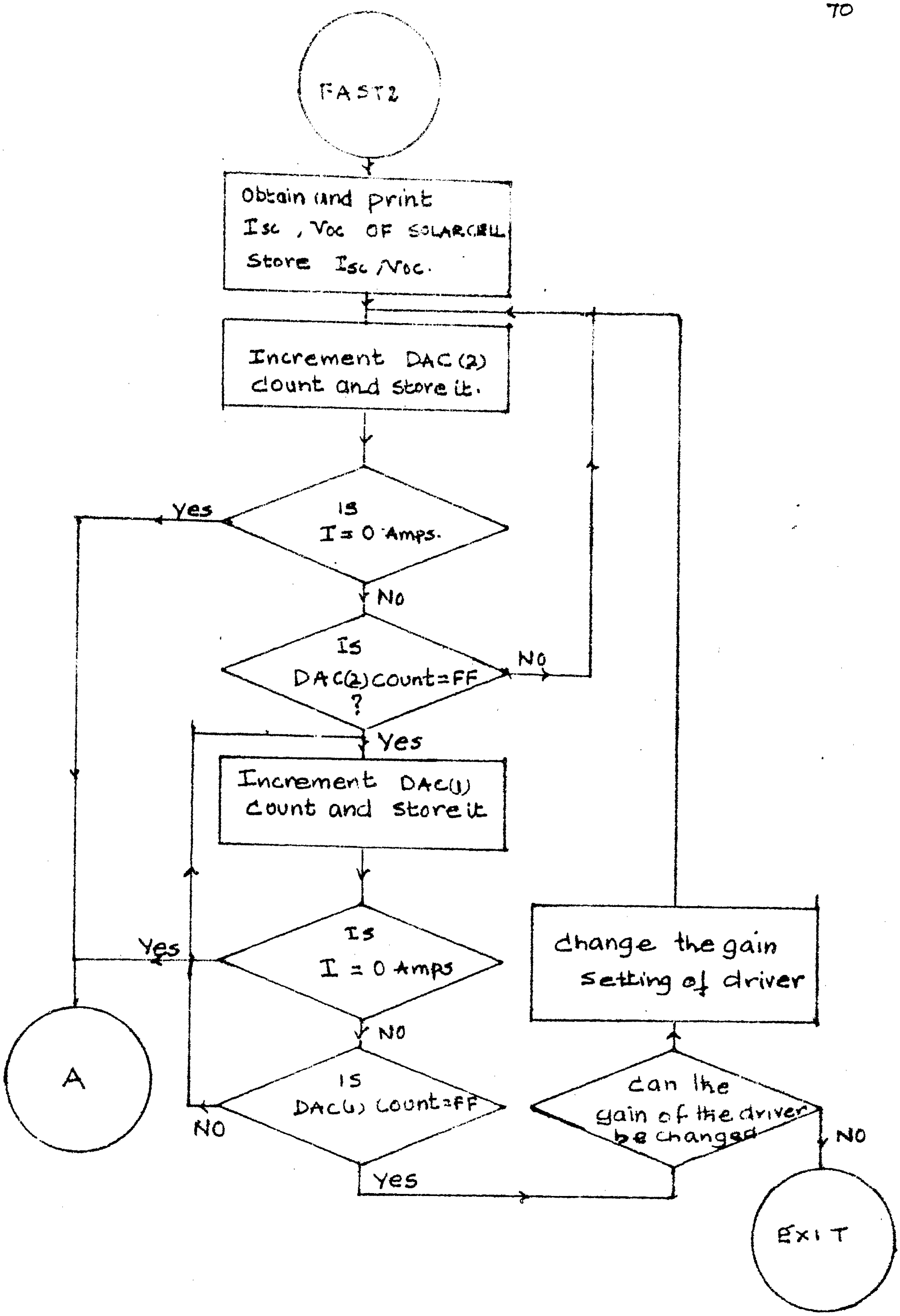
The whole test can be repeated for different illumination intensities.

The spectral response of the device can be studied if the required type of light excitation is made available.

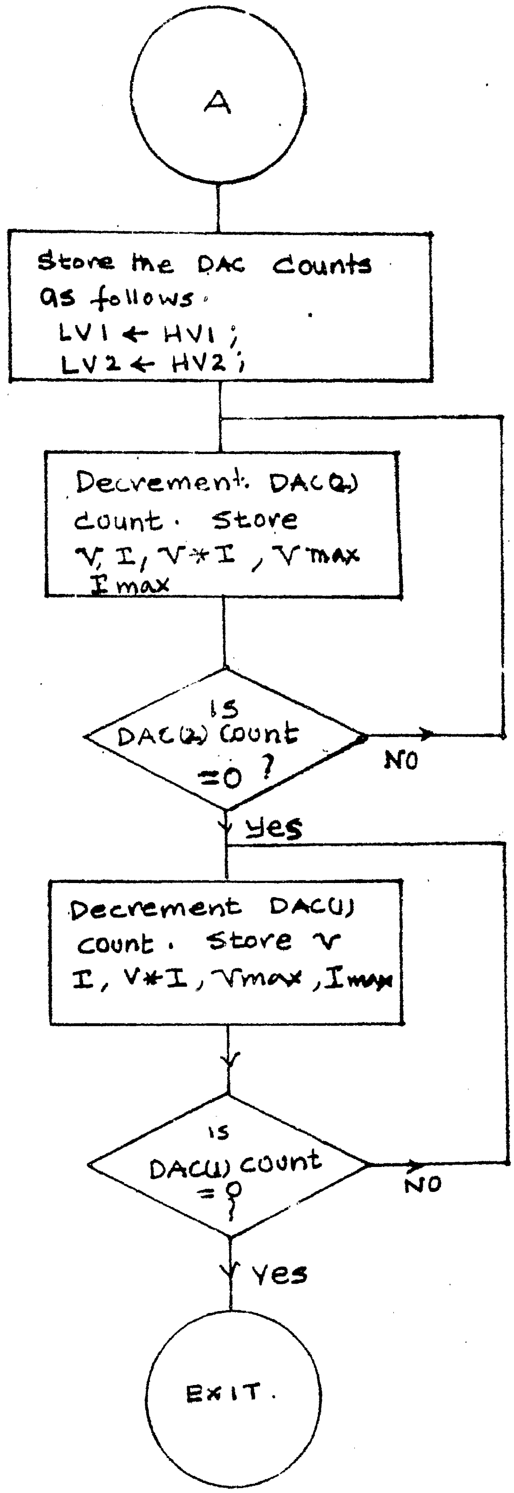
Step 7 : In a situation when DAC(1)-count = DAC(2)-count = FF and yet I≠0, the gain of the drive should be



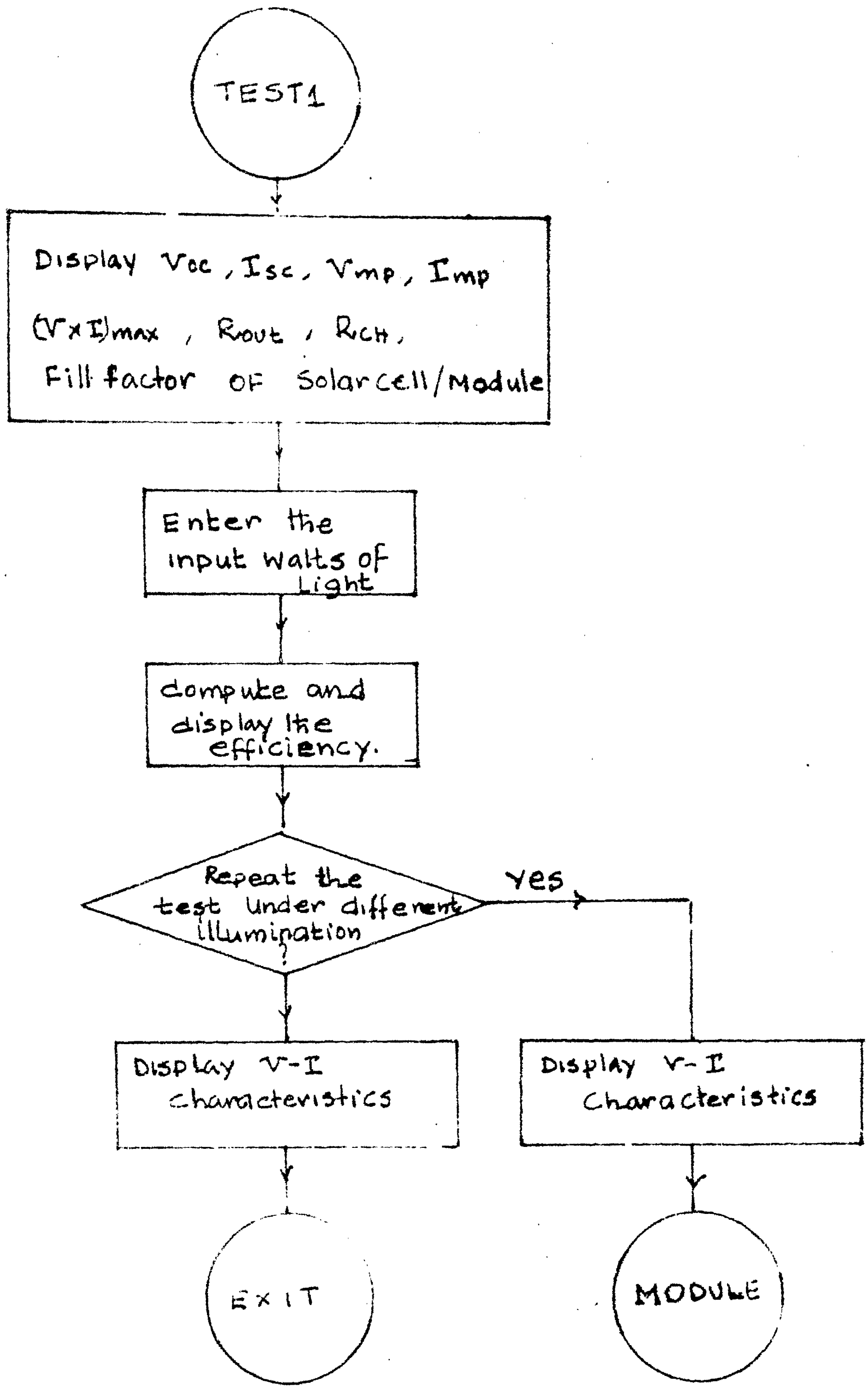
Flowchart-4 MODULE



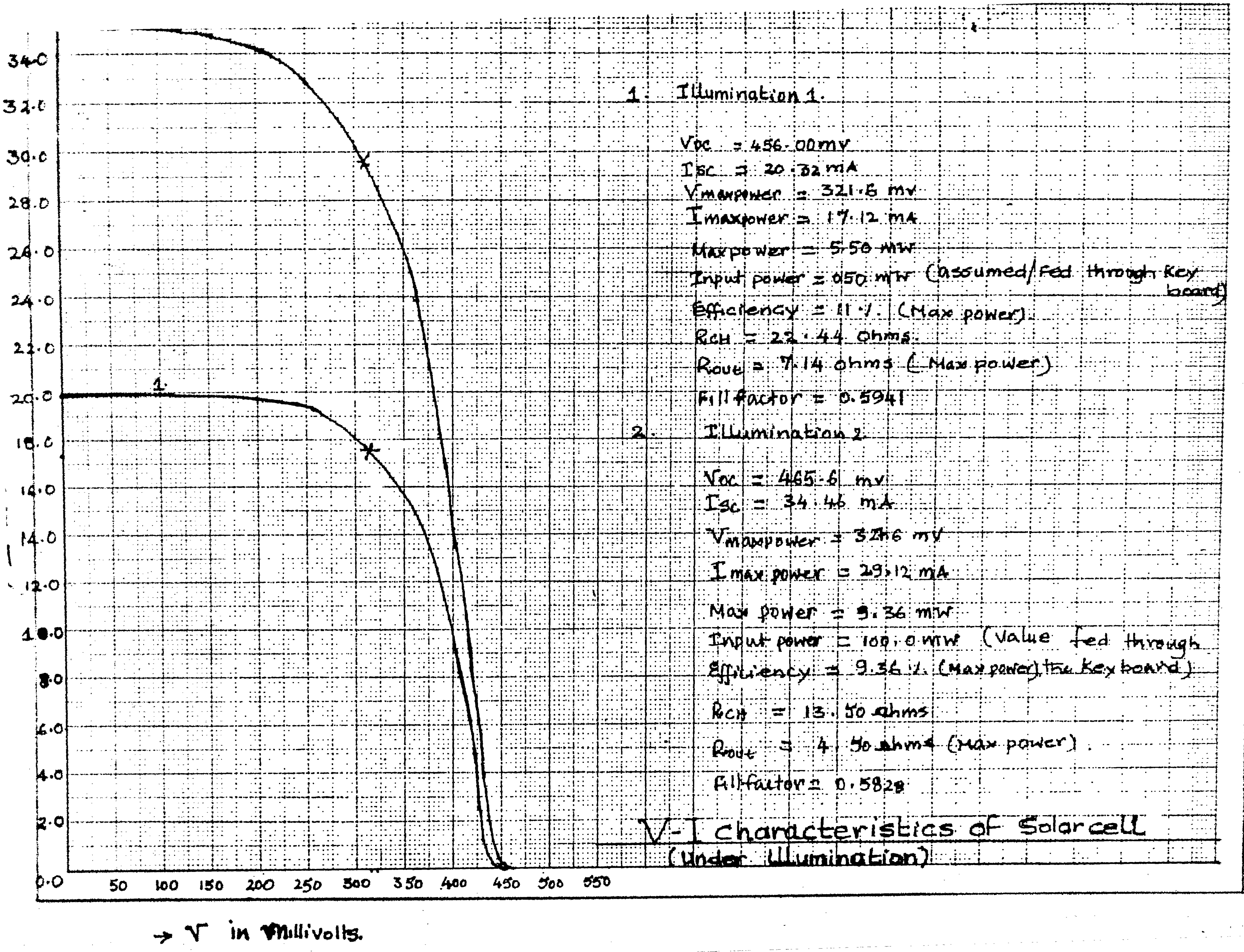
Flowchart.5 FAST 2



Flowchart 6 A (CONT OF FAST 2)



Flowchart·7 TEST1


34.0
32.0
30.0
28.0
26.0
24.0
22.0
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
50
100
150
200
250
300
350
400
450
500
550
1
1. Illumination 1.
Voc = 456.00 mV
Isc = 20.32 mA
Vmaxpower = 321.6 mV
Imaxpower = 17.12 mA
Maxpower = 5.50 mW
Input power = 050 mW (assumed/fed through key board)
Efficiency = 11 %. (Max power).
RCH = 22.44 ohms.
Rout = 7.14 ohms (Max power)
Fill factor = 0.5941
2. Illumination 2.
Voc = 465.6 mV
Isc = 34.46 mA
Vmaxpower = 326 mV
Imax power = 29.12 mA
Max power = 9.36 mW
Input power = 100.0 mW (Value fed through the key board)
Efficiency = 9.36 %. (Max power)
RCH = 13.50 ohms
Rout = 4.50 ohms (Max power)
Fill factor = 0.5828
V-I characteristics of Solarcell
(Under illumination)
→ V in Millivolts.

* SOLAR CELL V-I CHARACTERISTICS *

INATION - 1

456. 0 mv ; Isc = 20. 32 ma;

321. 6 mv ; Imp = 17. 12 ma ; FF = 0. 5941

22. 44 ohms ; Rs = 07. 14 ohms

att = 5. 50 mw ; I/P Watt = 50. 0 w ; n = 11. 00%

V (mv)	I (ma)	V (mv)	I (ma)
456. 0	00. 00	321. 6	17. 04
451. 2	00. 00	316. 8	17. 20
446. 4	00. 00	314. 4	17. 36
441. 4	00. 00	309. 6	17. 60
439. 2	00. 16	304. 8	17. 84
434. 2	00. 40	302. 4	17. 84
429. 6	01. 20	297. 6	17. 92
427. 2	02. 24	295. 6	18. 08
427. 4	03. 34	290. 4	18. 08
417. 6	04. 08	285. 6	18. 40
415. 2	05. 12	280. 8	18. 48
410. 2	06. 00	278. 4	18. 64
405. 6	06. 60	273. 6	18. 72
403. 2	07. 60	268. 8	18. 80
398. 4	08. 40	266. 4	18. 88
393. 6	09. 20	264. 0	18. 96
391. 2	09. 92	259. 2	19. 10
386. 2	10. 64	254. 4	19. 12
381. 6	11. 28	249. 6	19. 28
379. 2	11. 84	247. 2	19. 12
374. 4	12. 40	242. 4	19. 46
369. 6	12. 96	237. 6	19. 28
364. 8	13. 44	235. 2	19. 36
362. 4	13. 84	230. 4	19. 44
357. 6	14. 24	218. 4	19. 52
355. 2	14. 64	180. 0	19. 76
350. 4	15. 12	139. 2	19. 76
345. 6	15. 36	100. 8	19. 92
340. 8	15. 60	060. 0	19. 92
338. 4	16. 00	021. 6	20. 08
333. 4	16. 32	012. 0	20. 08
328. 8	16. 56	002. 4	20. 08
326. 4	16. 64	000. 0	20. 08

INATION -2

465.6 mv ;   Isc = 34.48 ma

327.6 mv ;   Imp = 29.12 ma ; FF = 0.5828

13.50 ohms; Rs = 04.50 ohms ;

09.36 mw; I/P = 100.0 mw ; n = 9.36 %

V (mv)	I (ma)	V (mv)	I (ma)
465.6	00.00	326.4	28.56
460.8	00.00	321.6	28.12
456.0	00.16	319.2	29.36
451.2	00.24	314.2	29.76
448.8	00.74	309.6	30.08
444.0	01.92	307.2	30.32
439.2	03.20	302.4	30.72
436.8	04.48	297.2	30.80
432.0	05.76	295.2	31.12
427.2	07.04	290.4	31.36
422.2	08.40	285.4	31.60
420.0	09.44	283.2	31.84
415.2	10.72	278.4	32.00
410.4	11.76	273.6	32.32
408.0	12.96	271.2	32.48
403.2	14.00	266.4	32.48
398.4	15.20	261.6	32.64
396.0	16.04	259.4	32.72
391.2	17.36	254.4	32.80
386.4	18.24	249.6	33.04
381.6	19.28	247.2	33.20
379.2	20.16	242.4	32.40
374.4	21.04	237.6	33.28
369.6	21.84	225.6	33.44
367.2	22.64	187.2	34.16
362.4	23.44	148.8	34.48
357.6	24.16	108.0	34.86
355.2	24.86	069.6	34.71
350.4	25.44	031.2	34.72
345.6	26.00	021.6	34.64
343.4	26.56	012.0	34.88
338.4	27.12	002.4	34.80
331.2	28.08	000.0	34.72

increased and the test is started from the beginning. If there is no provision for gain change exit and print the error message.

TEST : This routine performs the testing in the same sequence as that of Fast 2 except that in this case of the 4 samples/V and I counts are obtained. And, the average counts are obtained and stored. (sample results and plots are attached).

4.3 PN-JUNCTION DIODE TESTING

With the existing setup the PN Junction diode forward characteristics can be obtained.

The following is the sequence of steps executed during the test.

1. Initialize the system. Connect device and the XY plotter to the terminals marked device and X-Y.

   A series resistance of the order of 50-100 Ω ($\frac{1}{2}$ W) is connected to limit the current through the device (especially after the cut-in or breakdown point).

2. Start from V = 10, I = 00.

Increment the (course) DAC(1) input from 00 and sense the current at each step.

3. If the current = X (current at cut in) then go to step 4 or else go to step 2.

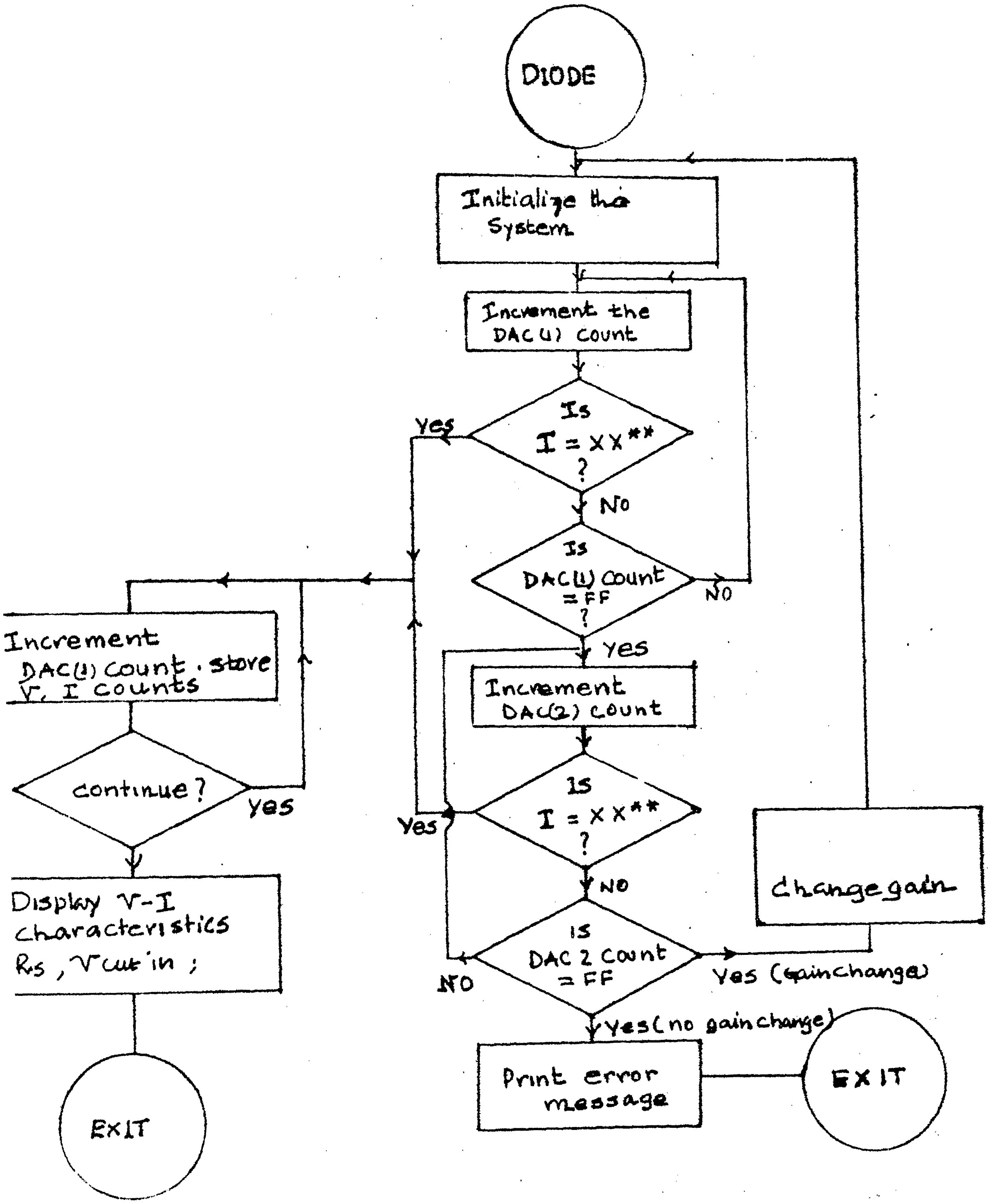
4. Now the V across the device corresponds to cut in voltage. The value of the V_{cut-in} is stored and displayed.

5. Now onwards the control will be transferred to user and the user decides the further action. He will have the options. He can either terminate the process or he can go further by a few steps (voltage increments on the curve) and again the choice is left to the user to either continue or to exit.

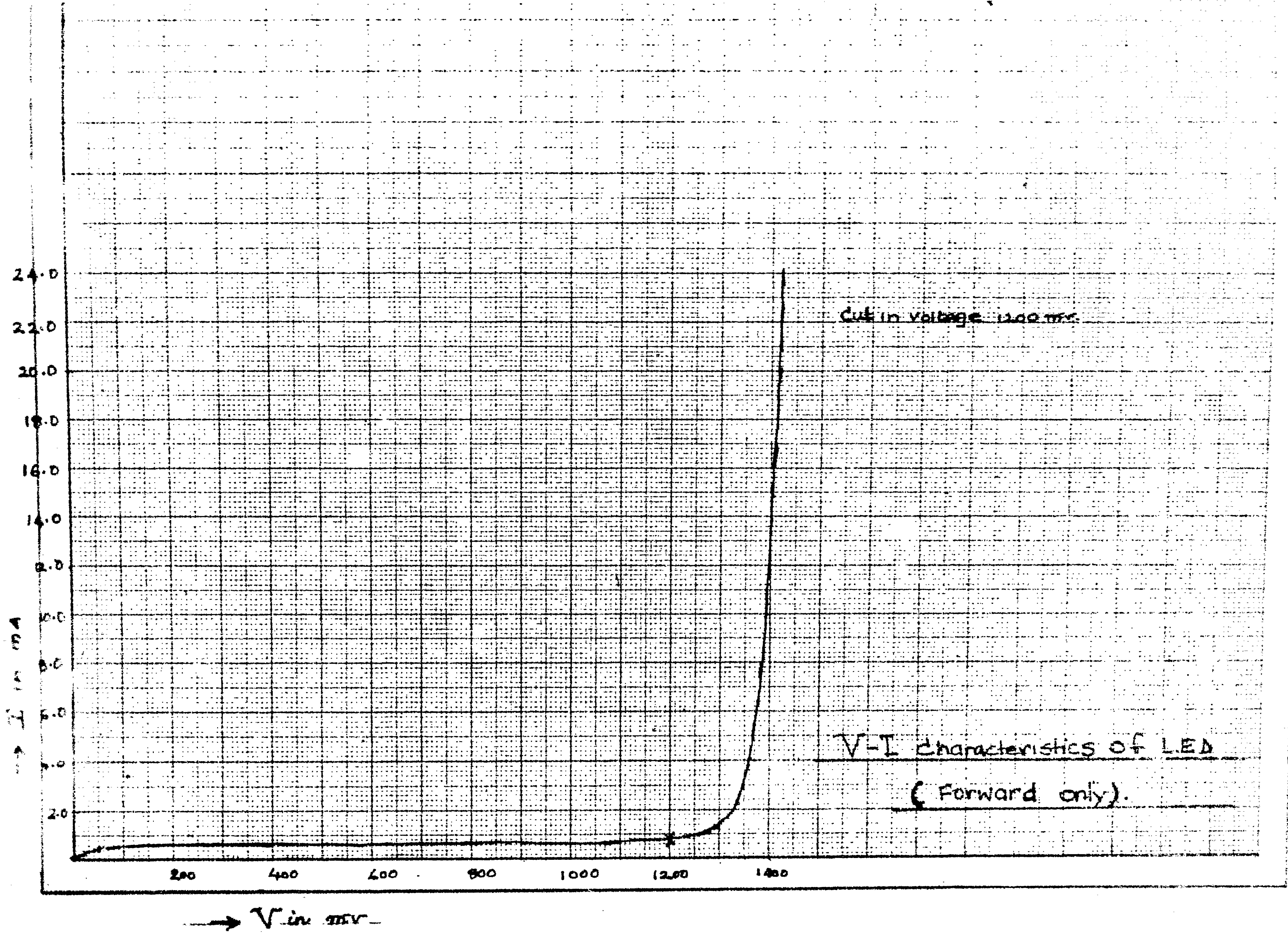
6. On the user's decision to exit, the XY plotter is disconnected and then, by entering the commands (as displayed on the screen) the V-I values are displayed.

The slope of the V-I curve is calculated and is displayed. The slope dV/dI gives an approximate value of the Resistance.

Once the cutin voltage is reached the control is trans-



Flowchart 8. DIODE



Cut in voltage 1200 mV
V-I characteristics of LED
(Forward only).
24.0
22.0
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
200
400
600
800
1000
1200
1400
→ V in mV
→ I in mA

V-I CHARACTERISTICS OF L E D

CUT IN V = 1200 mv

V (mv)	I (ma)
000.0	000.00
012.0	00.68
79.2	00.68
117.6	00.68
138.4	00.68
1024.0	00.68
1063.0	00.76
1104.0	00.78
1142.0	00.80
1180.0	00.84
1219.0	00.86
1262.0	01.00
1300.0	01.40
1308.0	01.64
1327.0	02.20
1344.0	03.00
1356.0	03.80
1365.0	04.68
1375.0	05.64
1382.0	06.68
1389.0	07.72
1396.0	08.76
1404.0	09.80
1408.0	10.84
1413.0	11.88

fered from DAC(1) to DAC(2), because from this point onwards the variation of I with V is large and hence a fine control over the voltage becomes necessary.

4.4 THREE TERMINAL DEVICE TESTING

In any three terminal device we have what are known as the main terminals which appear in the load circuit (in applications) and the control terminal which is third one. This, rather vague classification is important as far as our testing strategies are concerned.

Examples :

BJT - the collector and the emitter are the main terminals and the base is the control terminal

FET - the source and the drain are the main terminals and the gate is the control terminal

SCR - the anode and the cathode are main terminals and the gate is the control terminal.

To obtain the anode characteristics of the devices (the name of this characteristic may differ for different devices however), the control terminal voltage is kept constant (para-

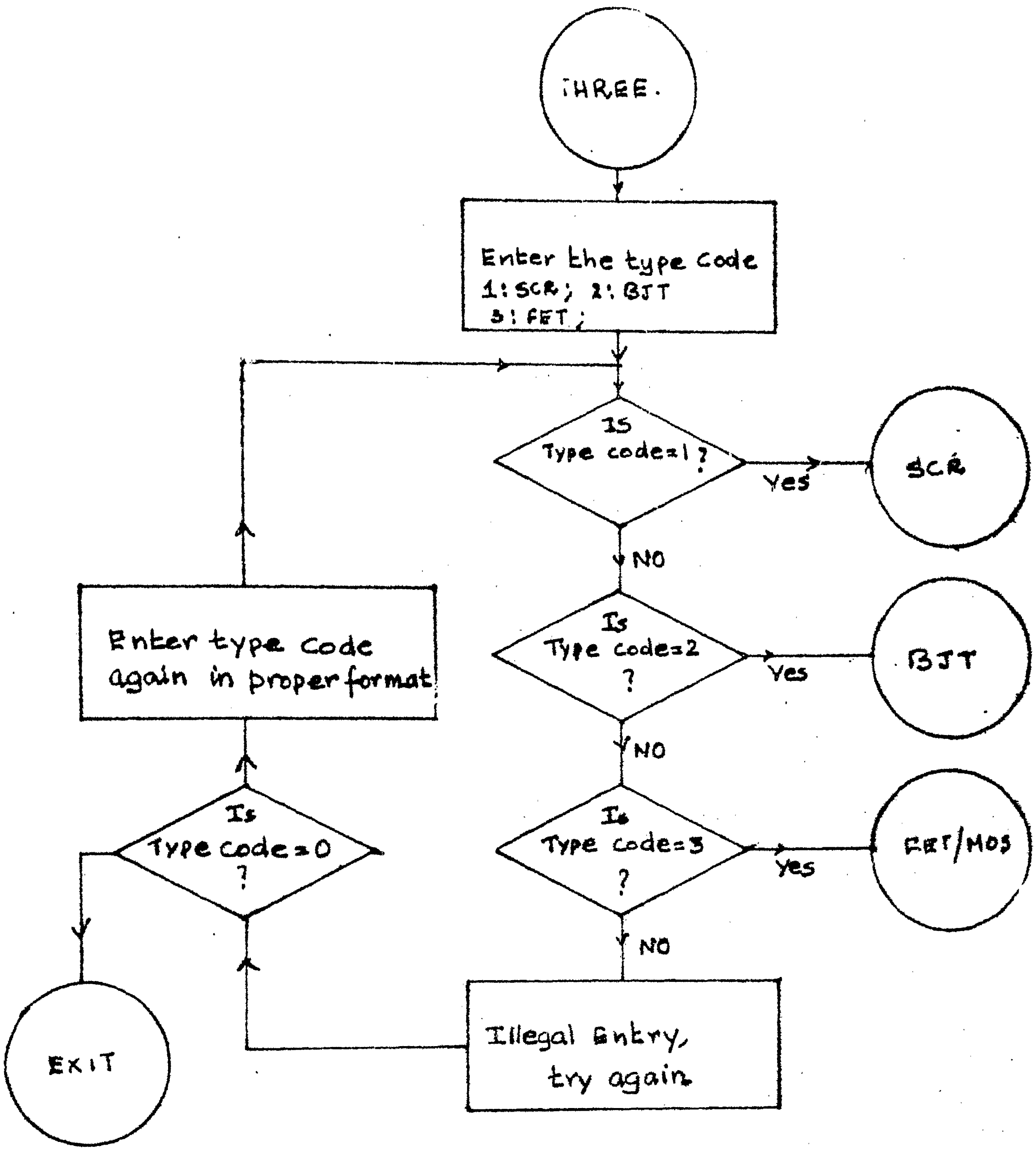
meter) and the variation of anode current with the variation of the anode voltage is studied. This test can be repeated for various values of control terminal voltage.

The main channel of the drive is used to drive the anode circuit and the second channel is used to drive the control terminal.

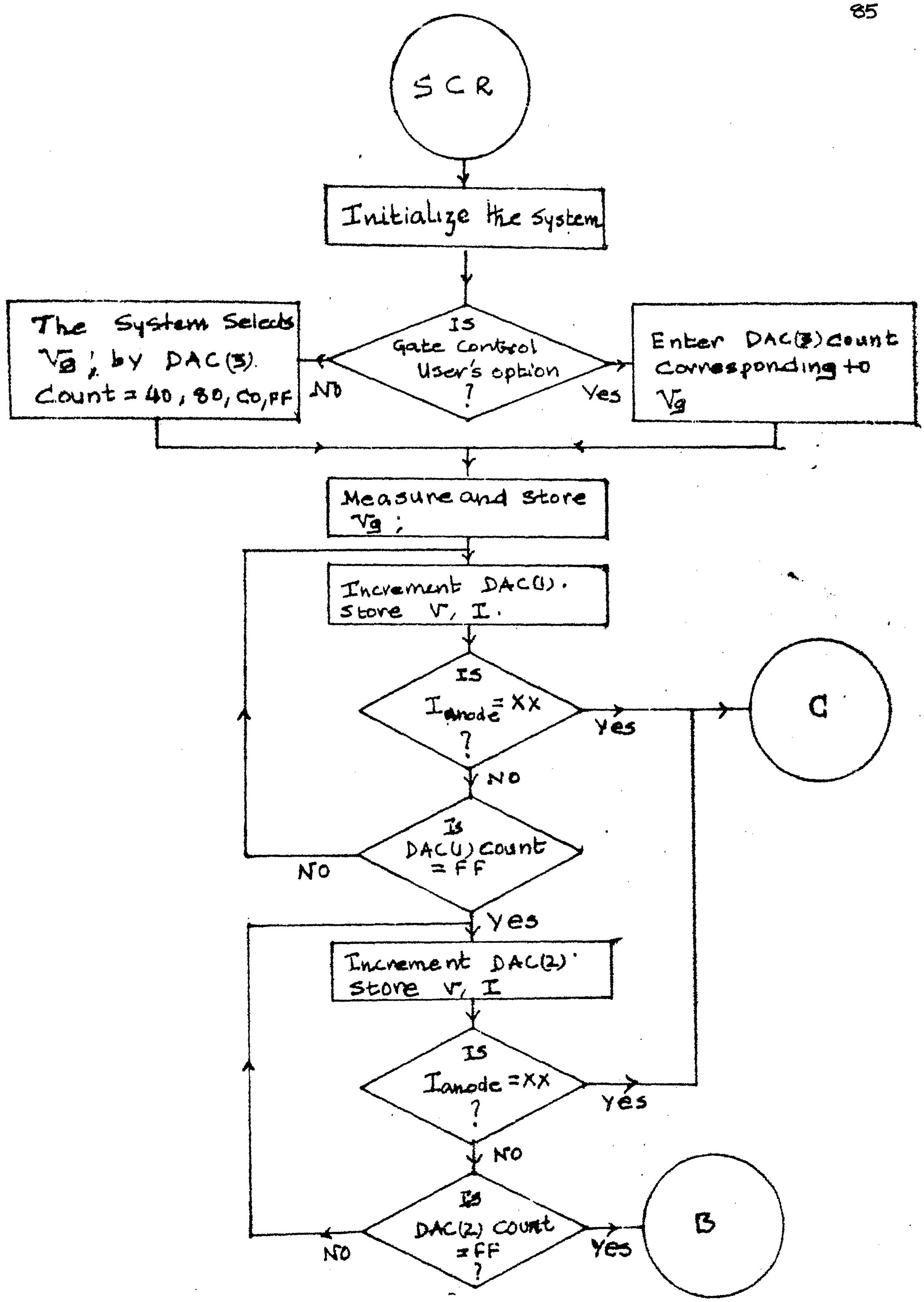
The more sensitive and less sensitive regions and the critical points etc. are handled in the same way as in the case of 2 terminal devices.

The program has been tested and it has worked satisfactorily for SCRs. The firing characteristics are obtained for different ranges of gate voltages.

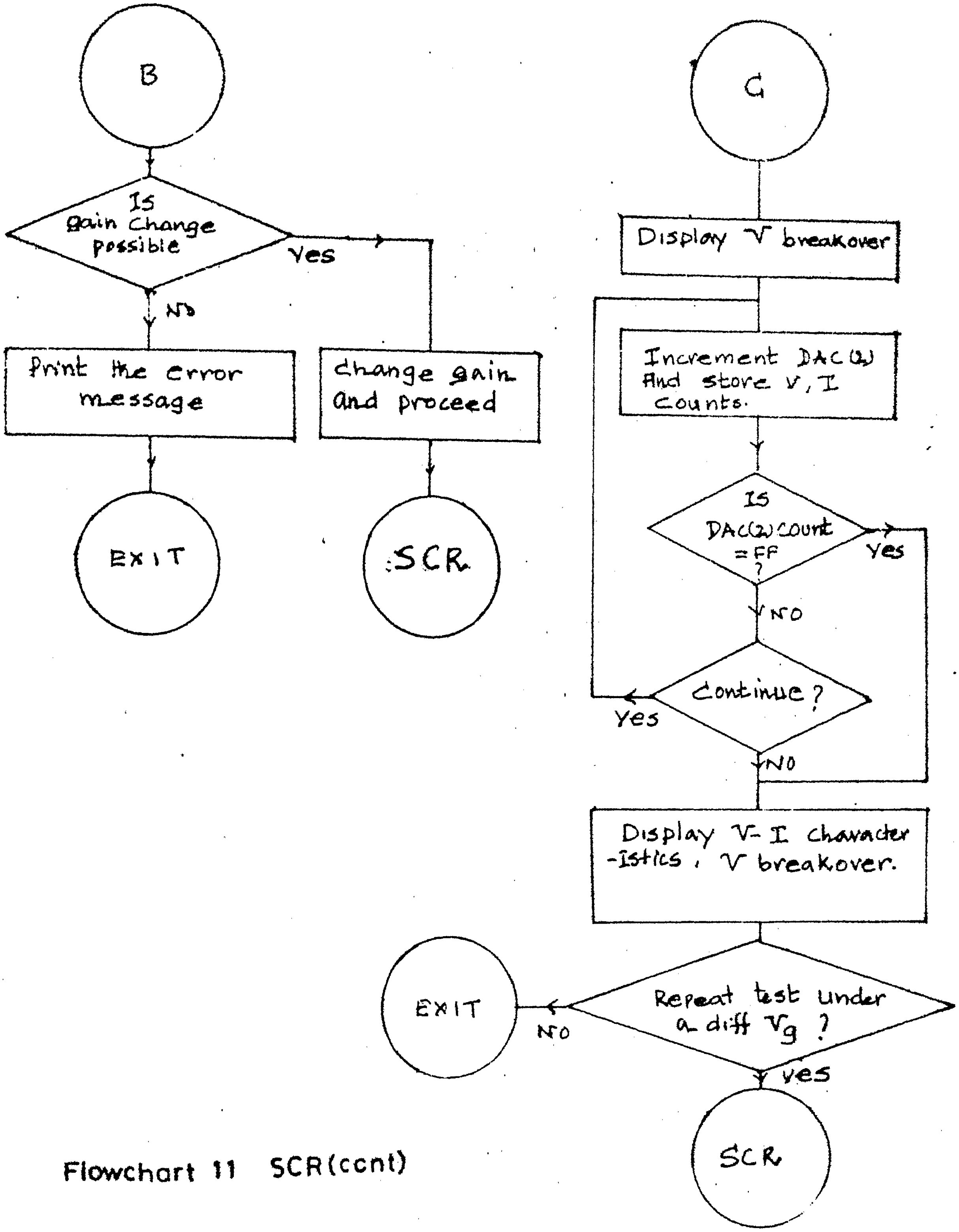
Note that even in the testing of 3 terminal devices it is the normal forward characteristics which is being obtained and not reverse characteristics.



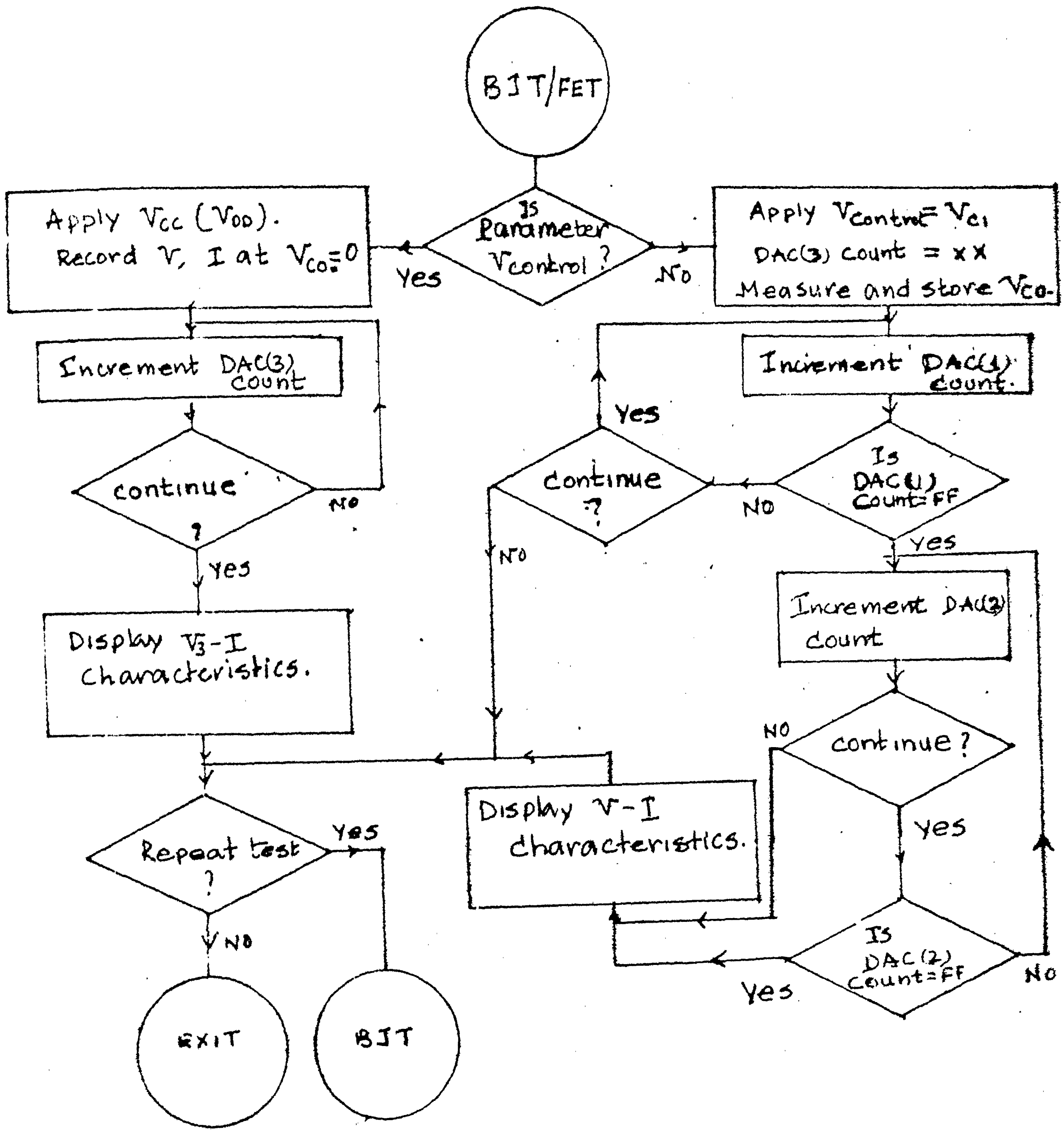
Flowchart·9 THREE



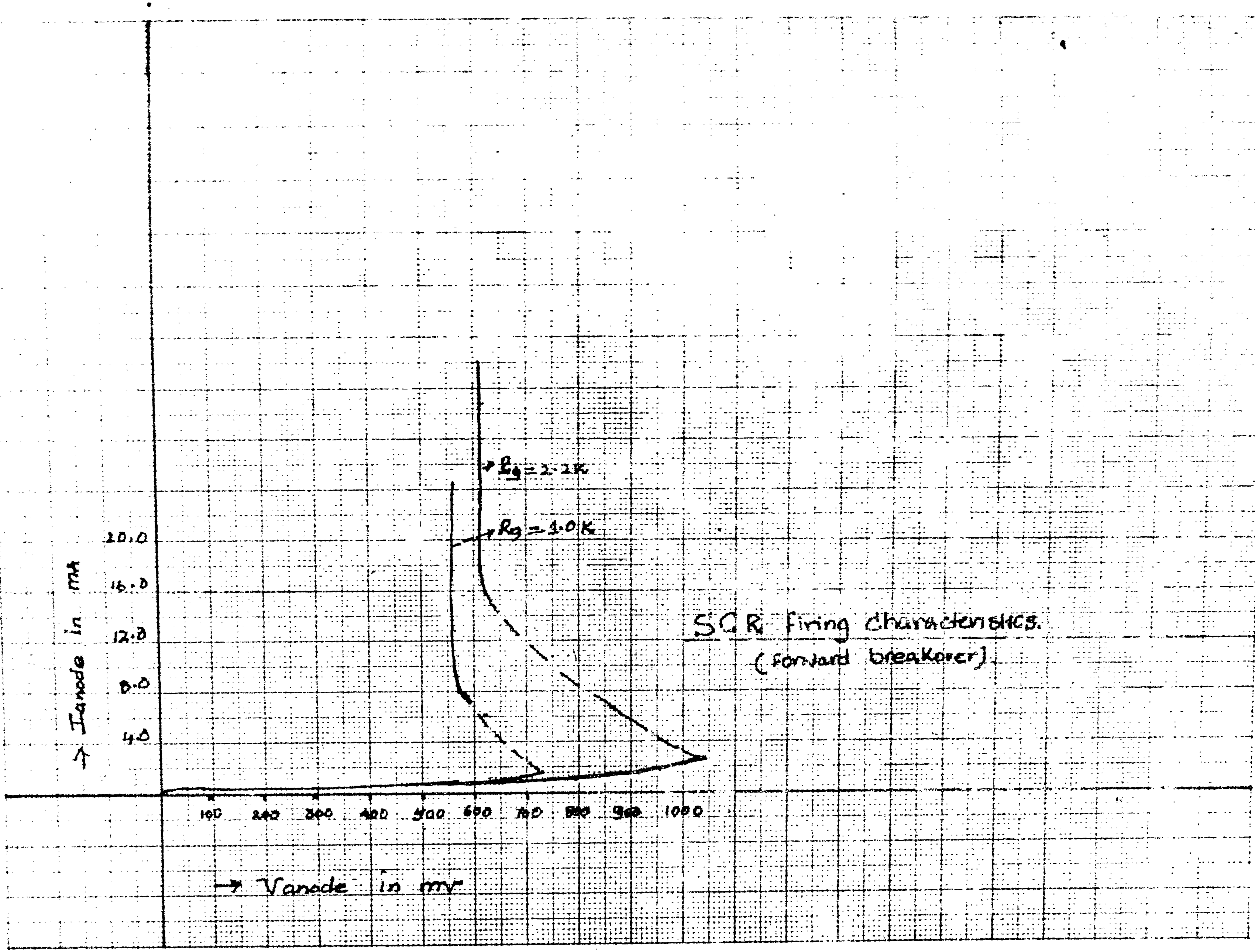
Flowchart ·10 SCR



Flowchart 11 SCR(cont)



Flowchart 12 BJT


SCR firing characteristics.
(forward breakover)
R_g = 2.2K
R_g = 1.0K
20.0
16.0
12.0
8.0
4.0
→ I_{anode} in mA
100
200
300
400
500
600
700
800
900
1000
→ V_{anode} in mV

V-I (FIRING) CHARACTERISTICS OF S C R

1 = 1K

V (mv)	I (ma)	
002.4	1.68	
012.0	1.68	
021.6	1.68	
079.2	1.68	
117.6	1.68	
158.4	1.68	
307.8	1.76	
482.4	1.84	
614.8	1.92	
722.4	2.00	
573.8	5.84	---------->break over
576.9	6.99	
576.[illegible]	8.00	

2 = 2.2K

V (mv)	I (ma)	
002.4	1.68	
012.0	1.68	
364.8	1.76	
631.2	1.84	
818.6	1.92	
1003.0	2.00	
1076.0	2.00	
609.0	16.80	---------->break down
612	17.36	
614.4	18.48	
614.8	18.80	

CHAPTER 5

CONCLUSIONS

5.1 OVERALL SYSTEM EVALUATION AND SUGGESTIONS FOR IMPROVEMENTS

A microcomputer based system has been developed for testing of semiconductor devices . It is intended to be the first step towards setting up of a computer aided device testing and characterization facility.

It has been possible with the present system to obtain static characteristics (with dc excitation) of various devices. With some additional software and hardware it should be possible for one to study the device's response to various forms of excitations, such as squarewave, triangular wave etc., which may be relevant. These waveforms can be easily generated with the help of the programmable timer and some additional wave shaping circuitry. In this kind of testing the speed of the system becomes a critical factor. The data converter circuits, buffers and other amplifiers used in such a set up must be fast enough to get any meaningful result .

In future implementations it is advised that faster and higher resolution DACs and ADC be used. Also the necessary waveform generating circuitry and the associated buffer circuits should be added to the present setup.

5.2 PROPOSED SCHEME FOR COMPUTER AIDED DEVICE TESTING FACILITY

Generalised methods for testing various semiconductor devices have been given in the form of flowcharts. The facility may be extended to test other devices which are presently not handled, by developing the necessary algorithm.

The programming would have been easier to develop and debug if the system were to support higher level languages. In a few years this may become more easily available on the micro-computer systems. A program developed in a higher level language will be portable, whereas the program written in an assembly language is not, since the assembly language is machine-dependent.

In future implementations it will be highly advisible to go for data acquisition modules which incorporate ADC, MUX, S/H and DAC etc. in one single chip. This helps

in improving the overall performance. The interfacing becomes simpler and elegant. The current buffers and current to voltage converters will have to be used to buffer the sub-system.

The device testing and characterization facility must include a floppy drive or cassette drive, a printer and graphic terminal interfaced to the system to make it a complete system (Fig. 5.1). Finally, it must be recognised that a system such as the one proposed should be made user friendly by incorporating extensive user interactive features.

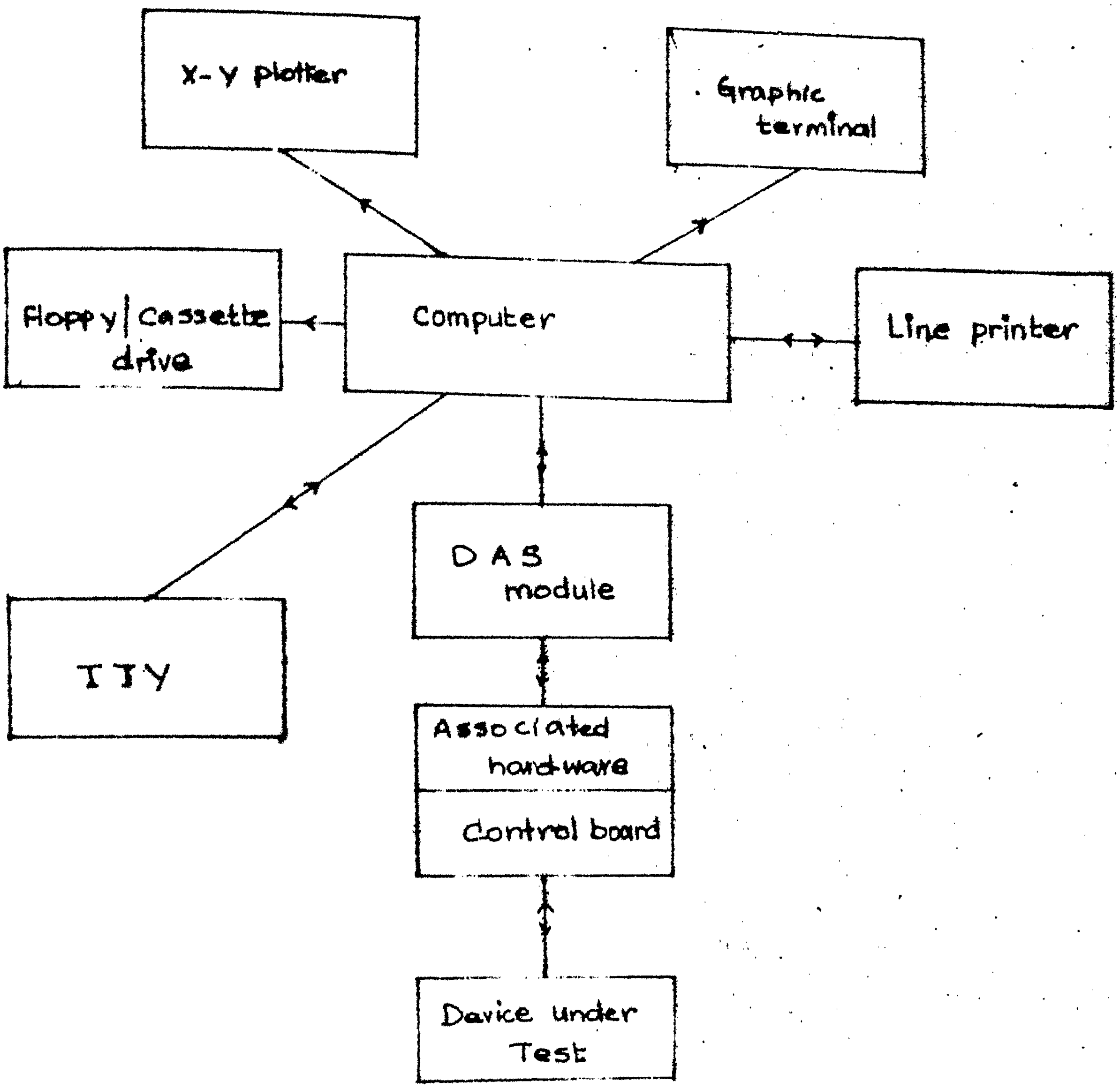


Fig 5.1 Computer Aided device testing facility

REFERENCES

1. Richard C. Jeager, 'Tutorial : Analog Data Acquisition Technology', Part I - 'Digital-to-Analog Converters' (IEEE Micro) Vol.2, No.2, May 1982, p.22.

   Part II - 'Analog-to-Digital Converters' Aug 1982, p.46.

   Part III - 'Sample and Holds, Instrumentation Amplifiers and Analog Multiplexer' Nov. 1982, p.20.

   Part IV - 'System Design, Analysis and Performance'. Feb. 1983, p. 52.

2. G. Aravanan, 'M.Tech. Thesis, Microcomputer based Solar Cell data acquisition System. July 1979.

3. Martin Green, 'Solar Cells'

4. Joseph J. carr, 'Micro Computer Interfacing ; Hand book of A/D and D/A Converters. TAB 1271.

5. Data Acquisition System Handbook - DATE-INTERSIL Co.

6. Intel 8085/A Family Data manual.

7. R. Schultz, et. al., 'A Microprocessor-based Solar Cell Test System', IEEE Trans. on Instrumentation and Measurement, Vol. IM-26, No.4, Dec. 1977.

APPENDIX A

It is often felt that for a system such as ours some documentation on handling and maintainence will be of great utility and importance. It is also important to provide some information on testing and calibration of individual functional modules. A brief write up on these topics is presented in the following few pages.

System Operation Sequence

It is important to note that for satisfactory working of the system, the system be installed in a airconditioned room or laboratory. We need a $\pm$ 12 V d.c. dual power supply.

The following sequence of operation should be followed strictly to ensure proper results.

1. Switch on the microcomputer and the power supply to the system simultaneously. Also connect the X-Y recorder to the terminals marked X-Y plotter and switch it on (see note on X-Y plotter).

2. The system responds with a message 'Terminal Ready Monitor Version X Y'. Now enter the following command through the

keyboard.

GO E000

3. On the execution of the above the system displays some messages regarding the system and instructions for the user. The system is then initialised.

4. The system now asks the user to select the device and the range through the keyboard by entering the device code. The format should be followed strictly. Otherwise, the system will respond with a message 'illegal entry, try again' and the needed information is to be provided.

5. Once the device is selected, the execution jumps to the corresponding routine. Follow the instructions displayed on the screen and enter the required data according to the specified format only. The device is connected after the system gives the appropriate message.

6. The process of testing is fully under the user's control and can be halted by pressing ^S (control S) and can be continued by pressing ^Q (control Q). The system can be reset by control C (^C). Note that the execution cannot be traced backwards but can only be halted and proceeded.

6. The X-Y recorder is switched off after the plot is obtained.

7. The results are displayed on user's request on the TTY screen. On completion of the test disconnect the device, switch off the XY plotter, power supply and the microcomputer.

Testing of Individual Functional Modules

Testing of Driver Circuit

The driver circuit consists of DACs, current buffers, voltage followers. Hence the testing of driver circuit is essentially testing of DAC_S, current buffers and the voltage followers.

A small program is executed to generate Sawtooth and staircase waveforms over the complete range of the DAC. The voltages are checked at the output of the DAC, voltage followers and at the output of the buffers. The offsets and errors, if any, are detected and the corrections necessary are made. Once the offsets are nulled, the setup is not disturbed until further testing and calibration.

The calibration process of the driver is basically that of a DAC. The input to the DAC is changed from 00 to FF

and at each increment the outputs of DAC, voltage follower and that of the buffer are adjusted to the correct value. The DAC gain is adjusted by trimming the reference input current. The outputs are measured by a precision digital voltmeter.

Testing of the Sensor Circuit :

The sensor circuit consists of ADC, MUX, S/H and the current to voltage converter.

The testing and calibration of the sensor circuit consists of applying known signals (reference currents) and checking for the outputs of the above said components and the output of ADC. Once the offset of ADC, MUX, S/H are all nulled the setup is not disturbed. Now the ADC is calibrated by trimming the gain (control pots) of the ADC reference circuit.

The calibration of the sensor and the driver can be verified together by connecting the output of the DAC to the input of S/H and then checking the corresponding output of the ADC.

MDS

The first step in the development of assembly language software is the definition of the problem. Once the problem is defined completely, flow charts are drawn to make the job of coding easier. Once the flow charts are drawn the coding is carried out. The program(s) is then assembled and the EPROM is programmed with the object code.

When the program length grows larger it is always advisable to go for subroutines, Micros etc to ease the task of program development. It becomes extremely difficult to hand-assemble the programs, which are long and hence the assembly is generally performed by a program known as assembler.

The assembly language program is entered and stored in the main memory of the MDS (or on floppy disk). Then the assembler program is invoked. The object code is now generated and may be stored on the floppy disk or the main memory.

Our MDS supports facility to develop software on higher level languages like FORTRAN 77, PASCAL, PL/M and assembly language of 8085, 8086 etc. It has a main memory and

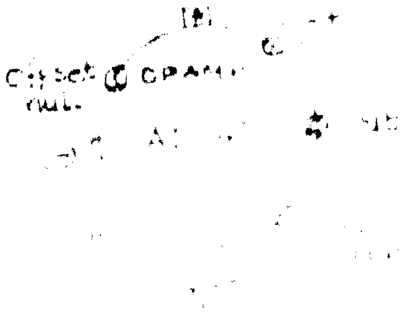
a secondary storage in the form of flexible disk on which our programs and the generated codes etc. are stored. The system programs are stored on a separate write-protected flexible disk.

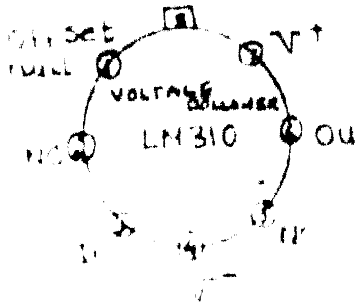
The MDS supports EPROM programming facility and a line printer besides the Incircuit-emulator. The EPROMS can be programmed and verified by the EPROM programming routine. It also permits selective programming and overlay The EPROMS should be fully erased by UV exposure. We have the necessary equipment for the same in the MDS laboratory.

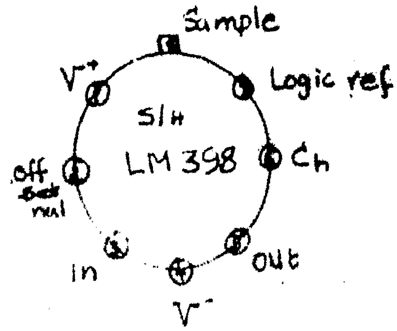
APPENDIX B

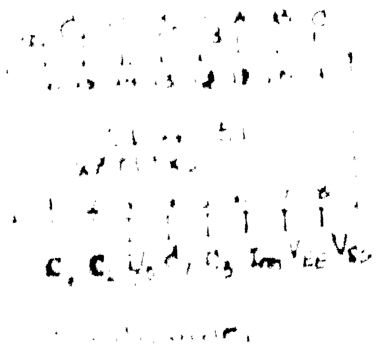
Pinout diagram of some I.Cs used in the system are given in this section.

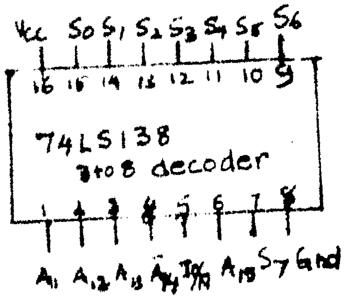
The block diagrams and pin-connections of 8255/A, 8253, and 2732A obtained from the Intel's manual are reproduced here for quick reference.


Offset null
OPAMP


Offset null
V+
VOLTAGE FOLLOWER
LM310
out
NC
V-


Sample
V+
Logic ref
S/H
LM398
off set null
Ch
in
out
V-


C1 C2


Vcc S0 S1 S2 S3 S4 S5 S6
16 15 14 13 12 11 10 9
74LS138
3 to 8 decoder
1 2 3 4 5 6 7 8
A11 A12 A13 A14 IO/M A15 S7 Gnd

8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel® Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easin
  Control Application Interface
- 40-Pin Dual In-Line Package
- Reduces System Package Count
- Improved DC Driving Capability

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It h 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the fir mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the secor mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for han shaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

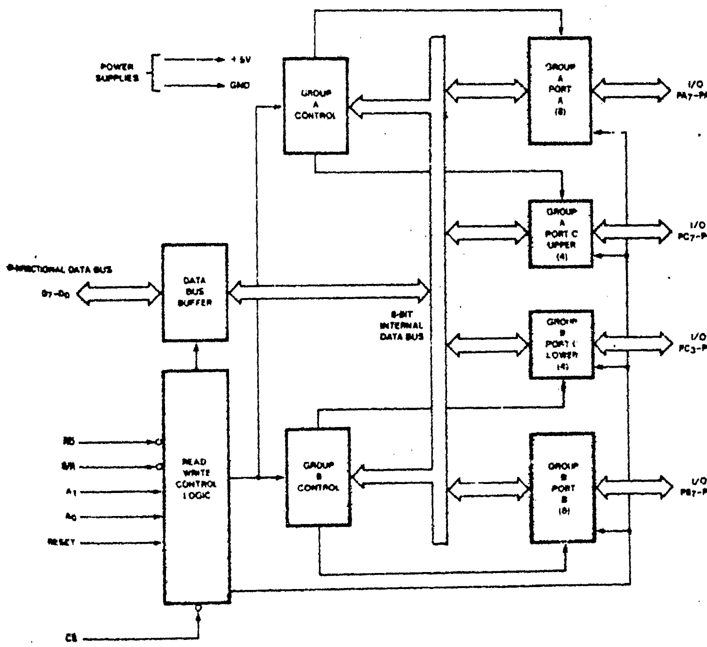


Figure 1. 8255A Block Diagram

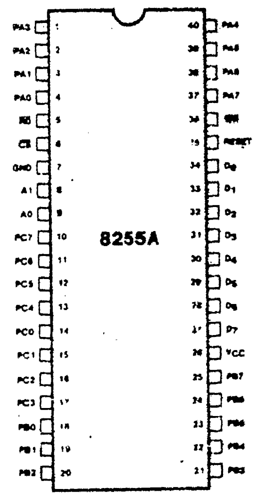


Figure 2. Pin Configuration

8253/8253-5
PROGRAMMABLE INTERVAL TIMER

- **MCS-85™ Compatible 8253-5**
- **3 Independent 16-Bit Counters**
- **DC to 2 MHz**
- **Programmable Counter Modes**
- **Count Binary or BCD**
- **Single +5V Supply**
- **24-Pin Dual In-Line Package**

The Intel® 8253 is a programmable counter/timer chip designed for use as an Intel microcomputer peripheral. It uses nMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

It is organized as 3 independent 16-bit counters, each with a count rate of up to 2 MHz. All modes of operation are software programmable.

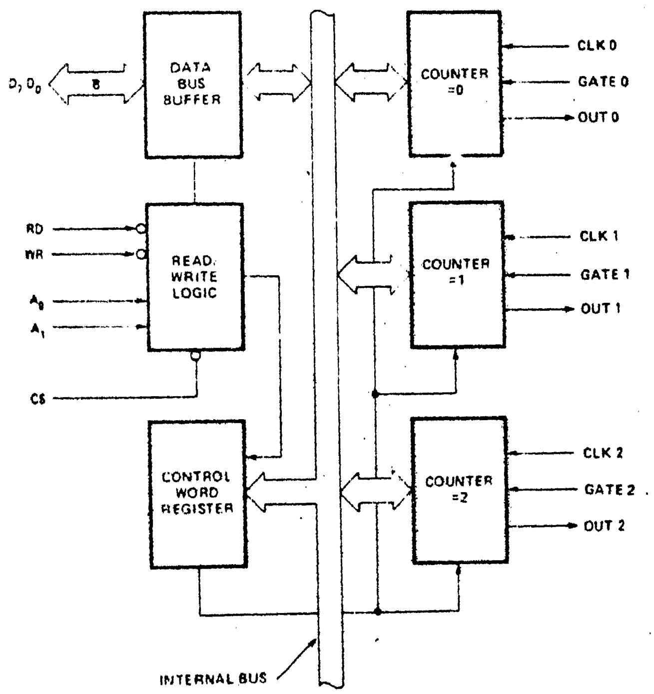


Figure 1. Block Diagram

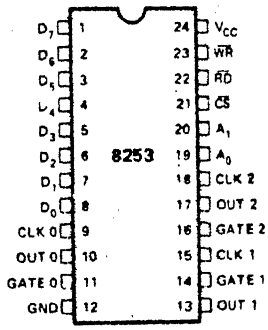


Figure 2. Pin Configuration

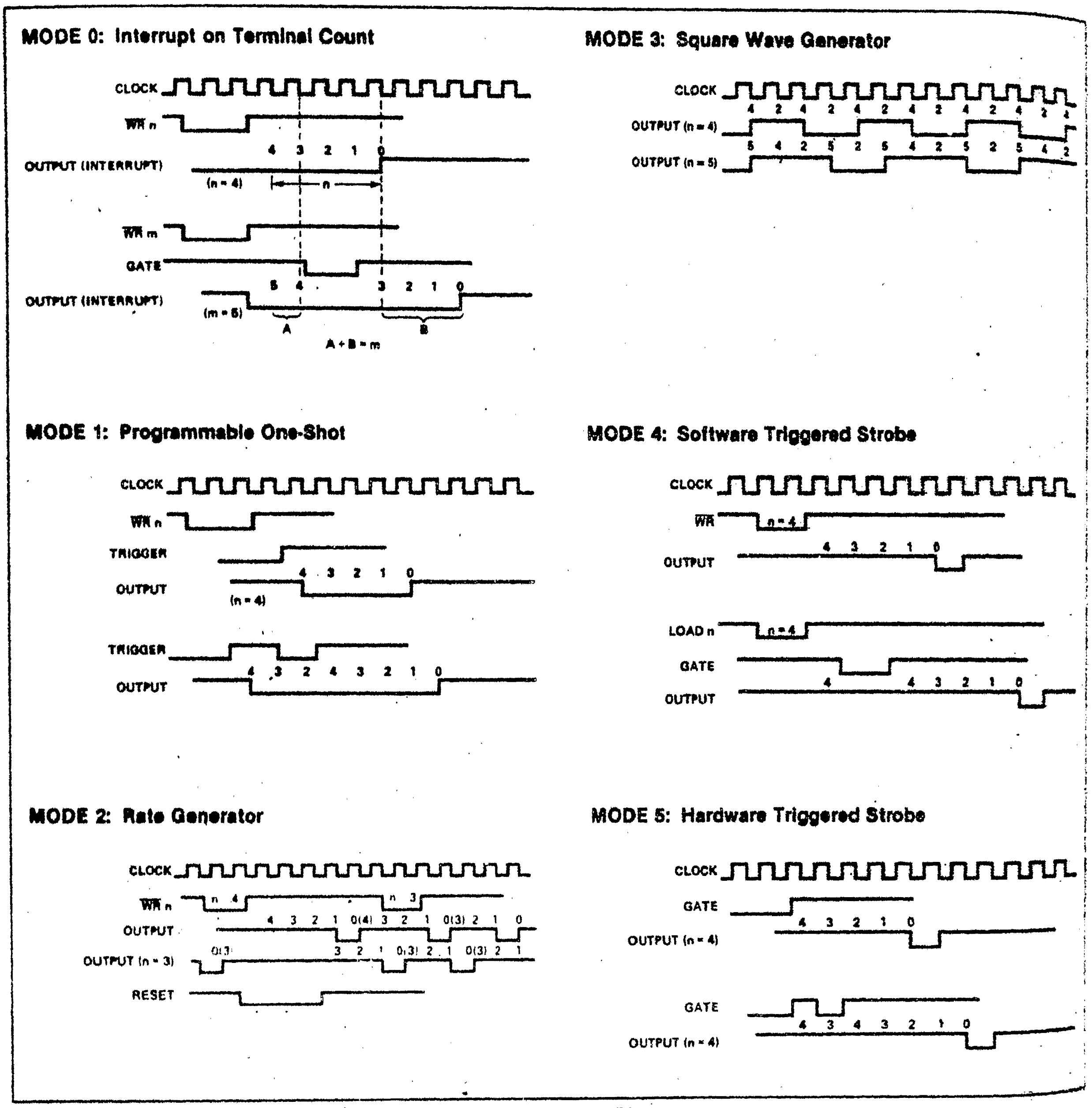


Figure 7. 8253 Timing Diagrams

2732A
32K (4K × 8) UV ERASABLE PROM

- 200ns (2732A-2) Maximum Access Time . . . HMOS*-E Technology
- Compatible to High Speed 8mHz 8086-2 MPU . . .Zero WAIT State
- Two Line Control
- Pin Compatible to 2764 EPROM
- Industry Standard Pinout . . . JEDE(Approved
- Low Standby Current . . . 35mA Ma:

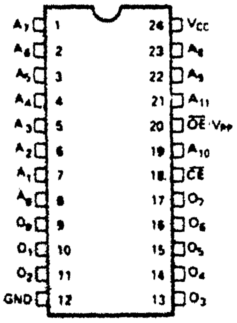
The Intel 2732A is a 5V only, 32,768 bit ultraviolet erasable and electrically programmable read-only memory (EPRC is pin compatible to Intel's 450ns 2732. The standard 2732A's access time is 250ns with speed selection (27: available at 200ns. The access time is compatible to high performance microprocessors, such as the 8mHz 808(these systems, the 2732A allows the microprocessor to operate without the addition of WAIT states.

An important 2732A feature is the separate output control, Output Enable ($\overline{OE}$), from the Chip Enable control ($\overline{CE}$). Th control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-72 describe microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's EPROMs. AP-72 is available from In Literature Department.

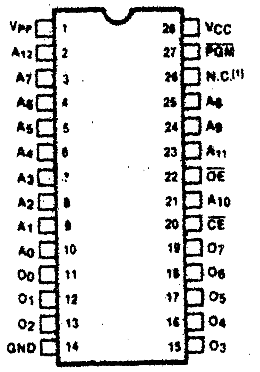
The 2732A has a standby mode which reduces the power dissipation without increasing access time. The maxi active current is 150mA, while the maximum standby current is only 35mA, a 75% saving. The standby mode is achi by applying a TTL-high signal to the $\overline{CE}$ input.

The 2732A is fabricated with HMOS*-E technology, Intel's high speed N-channel MOS Silicon Gate Technology.

2732A PIN CONFIGURATION



2764 PIN CONFIGURATION



[1]For total compatibility from 2732A provide a trace to pin 26

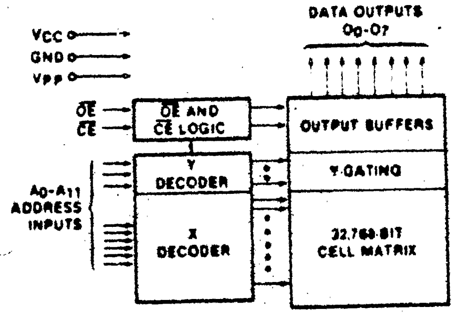
MODE SELECTION

PINS / MODE	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

PIN NAMES

A_0-A_{11}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

BLOCK DIAGRAM



*HMOS is a patented process of Intel Corporation.